Exhibit 3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner,

v.

SOLAS OLED, LTD.,
Patent Owner.

Case No. IPR2020-00320
U.S. Patent No. 7,446,338

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,446,338 UNDER 35 U.S.C. §§ 311–319 AND 37 C.F.R. § 42.100 *et seq.*

LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 7,446,338 (the "'338 patent")
1002	File History for U.S. Patent No. 7,446,338
1003	U.S. Patent Application Pub. No. 2002/0158835 ("Kobayashi")
1004	U.S. Patent Application Pub. No. 2004/0113873 ("Shirasaki")
1005	International Publication No. WO 03/079441 ("Childs")
1006	European Patent Application No. EP 1331666 ("Yamazaki")
1007	U.S. Patent Application Pub. No. 2004/0165003 ("Shirasaki II")
1008	Japanese Patent Publication No. 2004-258172
1009	U.S. Patent Application Pub. No. 2003/0151637 ("Nakamura")
1010	International Publication No. WO 03/079442 ("Hector")
1011	International Publication No. WO 03/079449 ("Young")
1012	Tsujimura, Takatoshi. *OLED Display Fundamentals and Applications: Fundamentals and Applications,* John Wiley & Sons, Incorporated, 2012. ("Tsujimura")
1013	Crawford, Gregory P. *Flexible flat panel display technology.* Vol. 3. West Sussex: Wiley, 2005. ("Crawford")
1014	U.S. Patent Application Pub. No. 2003/0127657 ("Park")
1015	U.S. Patent No. 7,498,733 ("Shimoda")
1016	U.S. Patent Application Pub. No. 2002/0000576 ("Inukai")
1017	U.S. Patent Application Pub. No. 2002/0009538 ("Arai")
1018	Declaration of Dr. Adam Fontecchio
1019	*Curriculum Vitae* of Adam Fontecchio

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I. INTRODUCTION

Samsung Display Co., Ltd. ("Petitioner") petitions for *inter partes* review seeking cancellation of claims 1–3 and 5–13 of U.S. Patent No. 7,446,338 (Ex. 1001, "'338 patent"), assigned to Solas OLED, Ltd. ("Patent Owner").

The '338 patent relates to active-matrix organic light-emitting diode (AMOLED) display panels. Ex. 1001, 1:51–65, 4:53–56, 5:51–53. The patent is directed to AMOLED displays having two purportedly distinctive features: (1) conductive "interconnections" that project from the surface of the substrate on which the OLED elements are formed, *id.*, 2:42–44, 3:63–67; and (2) a specific circuit to drive each pixel in the OLED device made up of three thin-film transistors ("TFTs"), *id.*, 6:45–7:18.

Regarding the first feature, the '338 patent describes and claims three types of projecting "interconnections" ("feed, "select," and "common"):

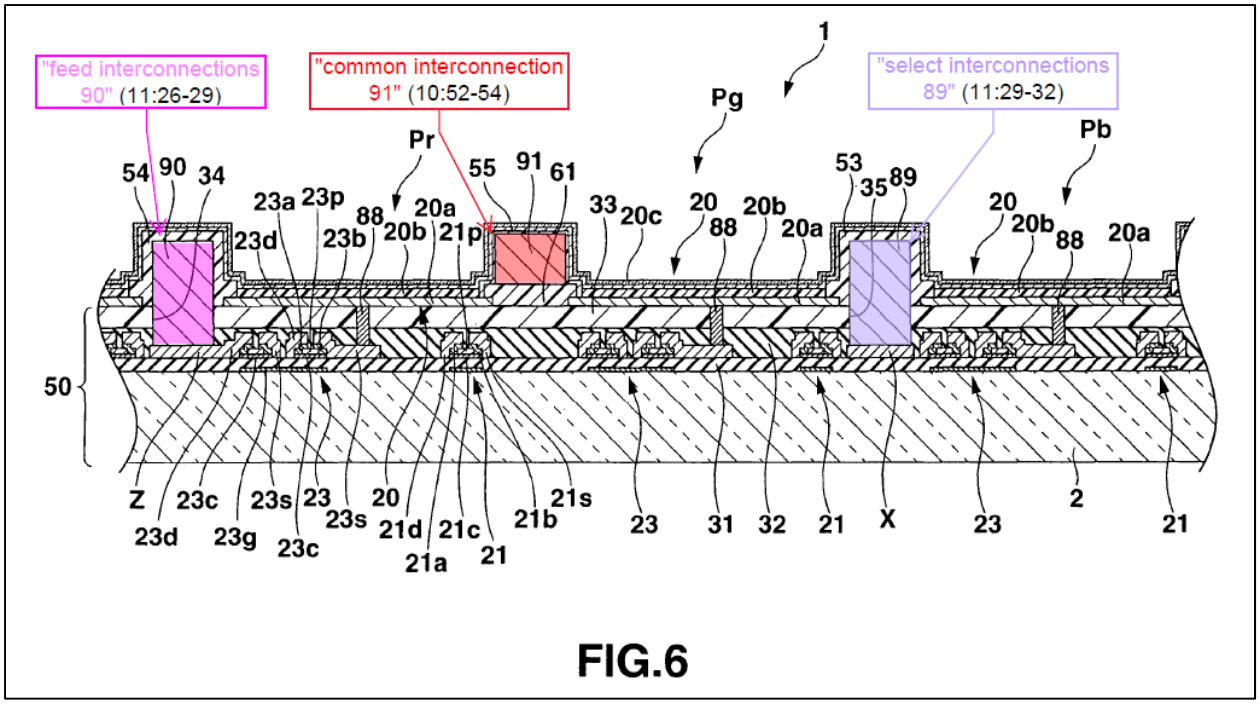


FIG.6

The ’338 patent explains that each type of interconnection is a low-resistance conductive element that “projects” upward in relation to the substrate below containing the TFTs (and on which the OLED elements are formed). *Id.*, 2:42–44. Each type of interconnection is electrically coupled to (and lowers the resistance of) a separate conductive component in the OLED structure. For example, the “feed” interconnection is electrically coupled to the voltage supply lines that bring power to the OLED elements, *id.*, 5:48–50, 14:20–29, and the “common” interconnection is electrically coupled to the transparent cathode electrode in each of the OLED elements, *id.*, 7:16–18, 17:59–18:7.

However, these types of projecting interconnections were all known in the prior art. Accordingly, during prosecution of the ’338 patent, original independent

claim 1 was rejected by the Examiner over the prior art. Ex. 1002, 446 (October 23, 2007 Non-Final Rejection) (citing "auxiliary electrode[s] 621" and "721" of European Patent Application No. EP 1331666 to Yamazaki et al. ("Yamazaki") (Ex. 1006) for the claimed "plurality of interconnections.").

To gain allowance of the '338 patent, the applicants added to independent claim 1 another feature—the specific three-transistor circuit structure of each pixel:

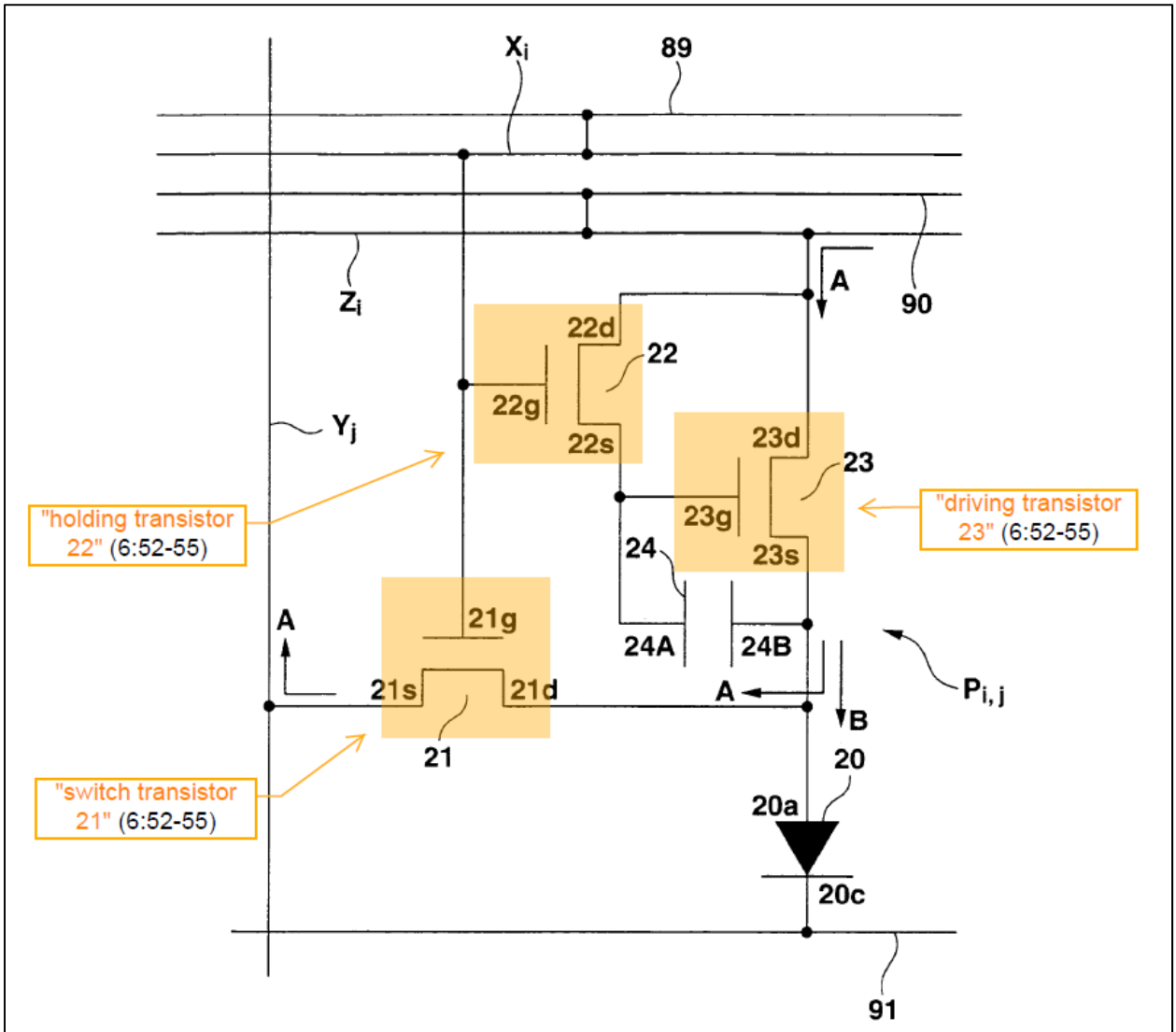


FIG.2

But while the Examiner believed this second feature to be novel at the time, he was not made aware that the prior art disclosed this specific structure and specifically encouraged use of it over two-transistor structures. For instance, the Examiner was not informed of prior art U.S. Patent Application Pub. No. 2004/0113873 to Shirasaki et al. ("Shirasaki"), which disclosed this three-transistor pixel circuit structure more than a year before the U.S. filing date of the '338 patent. This reference was not identified during prosecution, even though it had the same lead inventor as the '338 patent.[1]

Shirasaki taught the three-transistor pixel circuit structure claimed in the '338 patent, with circuit diagrams depicting the same structure as found in the '338 patent. *Compare* Ex. 1004, Figs. 1, 5A–B, 9A–B, *with* Ex. 1001, Fig. 2. Moreover, Shirasaki explained why its three-transistor pixel circuit structure was an improvement for OLED displays and should be used instead of the two-transistor pixel circuit structure more commonly used in OLED displays at the time. *See* Ex. 1004, ¶¶ [0002]–[0025].

[1] For clarity, because this prior art reference and the challenged patent share the same lead inventor, Tomoyuki Shirasaki, the Petition refers to this reference as "Shirasaki," and to the challenged patent as "the '338 patent."

Thus, both purportedly distinctive features of the ’338 patent were taught in the prior art as desirable features to improve the performance of OLED displays. Further, as noted above, Shirasaki described why it would have been beneficial to use its three-transistor pixel circuit (the second feature) to replace the conventional pixel circuits found in OLED prior art that included the claimed “interconnections” (the first feature). Accordingly, claims 1–3 and 5–13 would have been obvious to a person of ordinary skill at the time of the alleged invention based on the prior art.

As explained in Ground I below, claims 1–2, 5–6, and 9–11 are unpatentable over U.S. Patent Application Pub. No. 2002/0158835 to Kobayashi et al. (“Kobayashi”) in view of Shirasaki. Kobayashi teaches the claimed “common” type of projecting interconnections, which are electrically connected to and lower the resistance of the pixel cathode. The combination of Kobayashi and Shirasaki would have been no more than simple substitution of one known element (Shirasaki’s three-transistor pixel circuit) for another (Kobayashi’s two-transistor pixel circuit), a substitution motivated by the reasons expressly described by Shirasaki, Ex. 1004, ¶¶ [0002]–[0025].

As explained in Ground II below, claims 1–3 and 5–13 of the ’338 patent are unpatentable as obvious over the combination of International Publication No. WO 03/079441 to Childs et al. (“Childs”) and Shirasaki. Childs discloses the other two types of projecting interconnections claimed by the ’338 patent (“feed”

interconnections electrically connected to a supply line and "select" interconnections electrically connected to a scan line). Similar to the Kobayashi–Shirasaki combination, the combination of Childs and Shirasaki would have been no more than the simple substitution of Shirasaki's three-transistor pixel circuit for Childs' two-transistor pixel circuit, a substitution which again was motivated for the reasons described in Shirasaki, Ex. 1004, ¶¶ [0002]–[0025].

II. STANDING, MANDATORY NOTICES, AND FEE AUTHORIZATION

Grounds for Standing: Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '338 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the '338 patent on the grounds identified in this petition.

Real Party-in-Interest: Petitioner identifies Samsung Display Co., Ltd., Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. as real parties in interest.

Related Matters: Patent Owner has asserted the '338 patent in litigation against the real parties-in-interest in *Solas OLED Ltd. v. Samsung Display Co., Ltd., et al.*, Case No. 2:19-cv-00152-JRG (E.D. Tex.). Patent Owner has also asserted the '338 patent in litigation against Apple Inc. in *Solas OLED Ltd. v. Apple Inc.*, Case No. 6:19-cv-00527 (W.D. Tex.), and against Google Inc. in *Solas OLED Ltd. v. Google Inc.*, Case No. 6:10-cv-00515 (W.D. Tex.).

Lead and Back-Up Counsel: Petitioner designates David A. Garr (Reg. No. 74,932, dgarr@cov.com) as lead counsel and Grant D. Johnson (Reg. No. 69,915, gjohnson@cov.com) as back-up counsel, both of Covington & Burling LLP, One CityCenter, 850 Tenth Street, NW, Washington, DC 20001 (postal and hand delivery), telephone: 202-662-6000, facsimile: 202-662-6291.

Petitioner also designates Peter P. Chen (Reg. No. 39,631) as back-up counsel, of Covington & Burling LLP, 3000 El Camino Real, 5 Palo Alto Square, 10th Floor, Palo Alto, CA 94306 (postal and hand delivery), telephone: 650-632-4700, facsimile: 650-632-4800.

Service Information: Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail at the email addresses above and at Samsung-Solas@cov.com.

Fee Authorization: The Office is authorized to charge $30,500 ($15,500 request fee and $15,000 post-institution fee) for the fees set forth in 37 C.F.R. § 42.15(a) (as well as any additional fees that might be due) to Deposit Account No. 60-3160.

III. SUMMARY OF CHALLENGE

Petitioner requests IPR of claims 1–3 and 5–13 of the ’338 patent under 35 U.S.C. § 103 based on the following prior art combinations:

- ***Ground I:*** Claims 1–2, 5–6, and 9–11 are obvious over the combination of Kobayashi and Shirasaki.

- ***Ground II:*** Claims 1–3 and 5–13 are obvious over the combination of Childs and Shirasaki.

The '338 patent has a U.S. filing date of September 26, 2005, and claims priority to a Japanese application filed on September 29, 2004. Each of the asserted references is available as prior art under 35 U.S.C. § 102 (pre-AIA)[2], as shown in the following table.

Exhibit	Reference	Date(s)	Availability as Prior Art
Ex. 1003	U.S. Patent Application Pub. No. 2002/0158835 ("Kobayashi")	October 31, 2002 (published); April 19, 2002 (filed)	§§ 102 (a), (b), and (e)
Ex. 1004	U.S. Patent Application Pub. No. 2004/0113873 ("Shirasaki")	June 17, 2004 (published); September 16, 2003 (filed)	§ 102 (b)[3]
Ex. 1005	International Publication No. WO 03/079441 ("Childs")	Sept. 25, 2003 (published); Feb. 21, 2003 (filed)	§§ 102 (a), (b), and (e)

[2] Because the application for the '338 patent was filed prior to March 16, 2013, the pre-AIA conditions for patentability apply.

[3] Foreign priority is not applicable for Section 102(b). *See generally* MPEP § 2133.02.

IV. OVERVIEW OF THE '338 PATENT

The '338 patent (Ex. 1001) states that it "relates to a display panel using a light-emitting element," Ex. 1001, 1:14–15—specifically, to a "organic electroluminescent display panel of [the] active matrix driving type" (i.e. an "AMOLED"), *id.*, 1:51–65, 3:53–56, 5:51–53; Ex. 1018, ¶ [0054]. The challenged claims are directed to an AMOLED structure with two key features: (a) conductive "interconnections" that project from the surface of a substrate on which the OLED elements are formed, *id.*, 3:63–67; and (b) a specific circuit design for each pixel in the OLED display panel made up of three TFTs, *id.*, 6:45–7:18.

In particular, challenged independent claim 1 recites:

> 1. A display panel comprising:
>
> [a] a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain;
>
> [b] a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other;
>
> [c] a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate;
>
> [d] a plurality of light emitting layers formed on the pixel electrodes, respectively and

[e] a counter electrode which is stacked on the light-emitting layers,

[f] wherein said plurality of transistors for each pixel include [1] a driving transistor, one of the source and the drain of which is connected to the pixel electrode, [2] a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and [3] a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

The '338 patent concedes, in the "Description of the Related Art," Ex. 1001, 1:16–2:30, that many of these claim elements were known in the art and commonly used in "conventional organic electroluminescent display panel[s] of [the] active matrix driving type," *id.*, 1:21–26, 1:51–52, noting that such conventional AMOLED display panels contained a "transistor array substrate" (element [a]), *id.*, 2:17–21; "an organic electroluminescent element . . . for each pixel" (elements [c]–[e]), *id.*, 1:24–31; "interconnections such as a power supply line," (element [b]), *id.*, 1:51–56; and "driving" and "switching transistors" (elements [f][1] and [f][2]), *id.*, 1:21–31; Ex. 1018, ¶ [0055].

The only purportedly novel elements of challenged independent claim 1 are the ones underlined above: that is, the claimed "interconnections which are formed to project from a surface of the transistor array substrate" (element [b]); and a three-transistor circuit "for each pixel" that includes a "holding transistor" in addition to

the conventional "driving and "switch transistor[s]" (element [f][3]). These features are discussed in the following two subsections.

A. "Interconnections Which Are Formed to Project from a Surface of the Transistor Array Substrate"

The '338 patent explains that in conventional AMOLED displays, electrical "interconnections such as a power supply line to supply a current to an organic EL element are patterned simultaneously in the thin-film transistor patterning step by using the [same] material as a thin-film transistor." Ex. 1001, 1:51–65. Because the electrical interconnections are formed in the same layer as the TFT, "the thickness of the interconnection equals that of the thin-film transistor," *id.*, which "is thin literally," *id.*, 2:2–3; Ex. 1018, ¶ [0056].

The '338 patent explains that these thin interconnections cause resistance problems: when "a current is supplied from the interconnection to a plurality of light-emitting elements, a voltage drop occurs, or the current flow through the interconnection delays due to the electrical resistance of the interconnection." Ex. 1001, 2:3–7. The '338 patent explains that other thin elements in conventional OLEDs similarly suffer from issues caused by high resistance—specifically, the cathode electrodes of the "organic EL element" itself, which are "[c]onventionally . . . formed as a transparent electrode of, e.g., a metal oxide having a high resistance value," such as "ITO [indium tin oxide]." *Id.*, 13:28–14:2. The "only" way to "sufficiently reduce the sheet resistance" of these transparent cathodes is "by

increasing the[ir] thickness," *id*, 14:2–3—but "[w]hen the material is thick, the transparency of the organic EL element decreases inevitably . . . and the display characteristic becomes poor," *id.*, 14:4–7; Ex. 1018, ¶ [0057].

To solve the problems caused by the high resistance of these components, the '338 patent proposes the use of three types of additional "interconnections," each of which has a "low resistance" and is "electrically connected" to higher-resistance components in the OLED structure (decreasing their resistance). Ex. 1001, 21:63–22:61. The "common interconnection" is electrically connected to the higher-resistance cathode electrode of the OLED elements, bringing down the resistance of that cathode and making its voltage "uniform[]" across the electrode. *Id.*, 22:2–10. Two other types of interconnections, "select" and "feed," are "electrically connected" to the "thin scan lines" and "thin supply lines" of the OLED display, respectively, bringing down the resistance of those thin lines. *Id.*, 22:20–61. The '338 patent explains that "[w]hen the resistance of these interconnections decreases, the signal delay and voltage drop can be suppressed." *Id.*, 3:63–67; Ex. 1018, ¶ [0058].

The '338 patent's "plurality of interconnections" are illustrated in annotated Figure 1, showing "a schematic plan view . . . of a display panel 1 which is operated by the active matrix driving method." Ex. 1001, 4:53–56. The display panel includes "a plurality of select interconnections 89, a plurality of feed interconnections 90, and a plurality of common interconnections 91," *id.*, 5:23–27,

arranged between "sub-pixel[s]" Pr, Pg, and Pb, *id.*, where "the select interconnection 89 overlaps" and is "electrically connected to the scan line [X]," and "[t]he feed interconnection 90 overlaps" and is "electrically connected to the supply line [Z]," *id.*, 5:46–50; Ex. 1018, ¶¶ [0059]–[0060]:

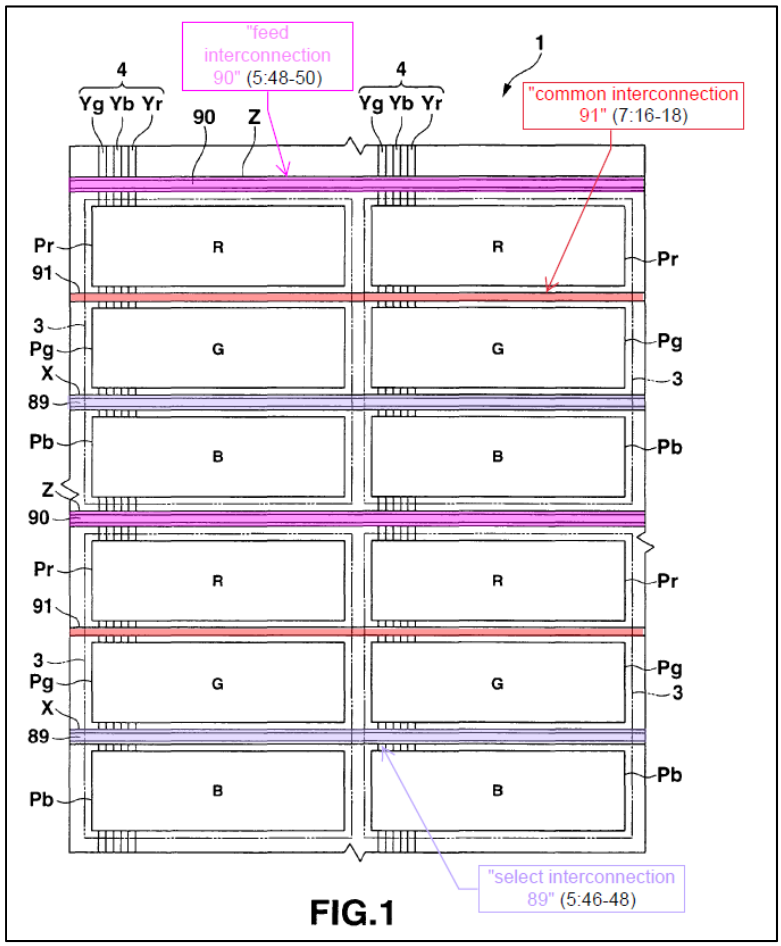


FIG.1

Figure 6 illustrates a cross-section of "the layer structure of display panel 1." Ex. 1001, 8:18–20. As this figure shows, the projecting interconnections are formed on top of a layered "transistor array substrate 50" (shown in orange). *Id.*, 10:42–47 (depicting "insulating substrate 2," "gate insulating film 31," "protective insulating film 31," and "planarization film 3" forming a "layered structure" that contains

"switch transistors 21" and "driving transistors 23" and "is called a transistor array substrate 50"); Ex. 1018, ¶¶ [0061]–[0062]:

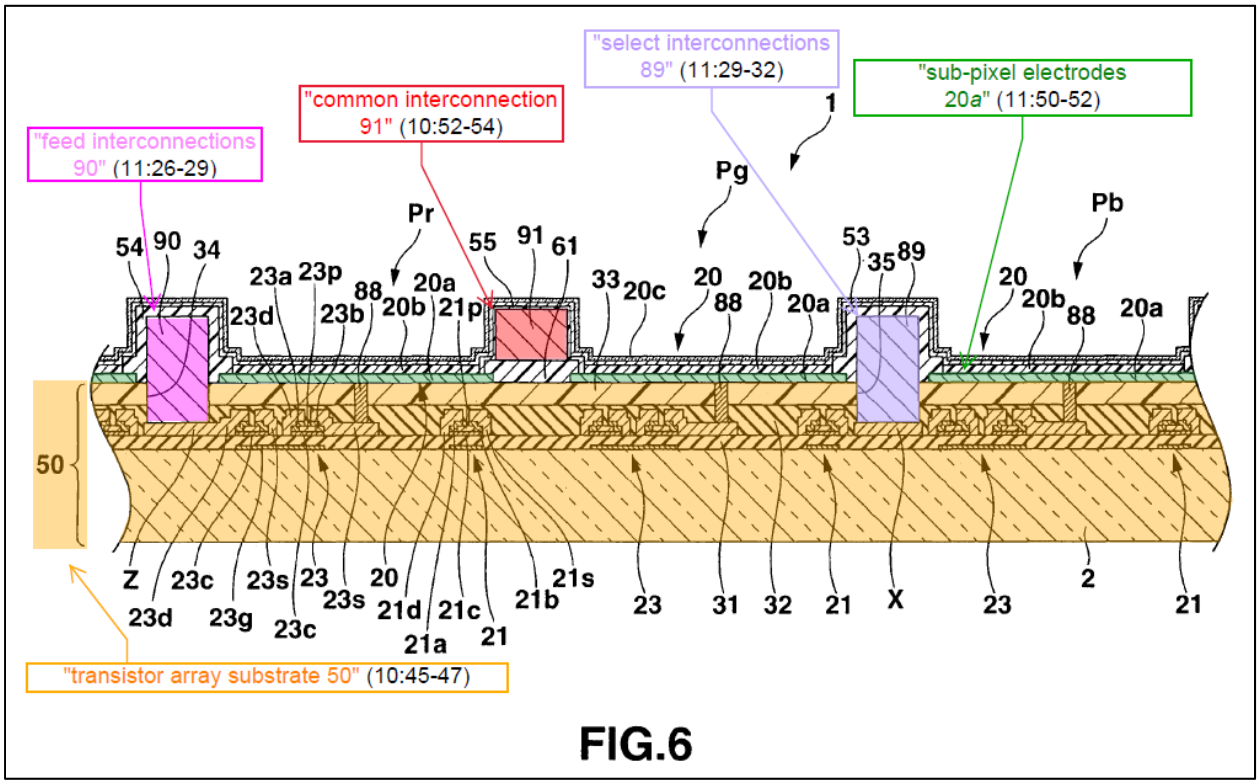


FIG.6

As illustrated in annotated Figure 6 above, "the select interconnection 89 and feed interconnection 90 project upward from the upper surface of the planarization film," Ex. 1001, 11:36–41, as does "common interconnection 91," which is "formed on the insulating line 61," *id.*, 10:48–58. Each of the "organic EL element[s] 20" is "electrically connected to the . . . source 23s of the driving transistor 23" through "contact hole 88," *id.*, 12:6–15, and the "counter electrode 20c functioning as the cathode of the organic EL element 20" is "electrically connected to the common interconnections 91," *id.*, 13:28–37; Ex. 1018, ¶ [0063].

B. "Driving Transistor," "Switch Transistor," and "Holding Transistor"

The "layered structure" of "transistor array substrate 50" includes within it three transistors for each sub-pixel of the display panel 1: "switch transistor 21," "holding transistor 22," and "driving transistor 23." Ex. 1001, 10:25–47. The "circuit arrangement" of these three transistors (along with interconnections 89–91 and organic EL element 20) is depicted in annotated Figure 2, *id.*, 6:45–7:18; Ex. 1018, ¶ [0064]:

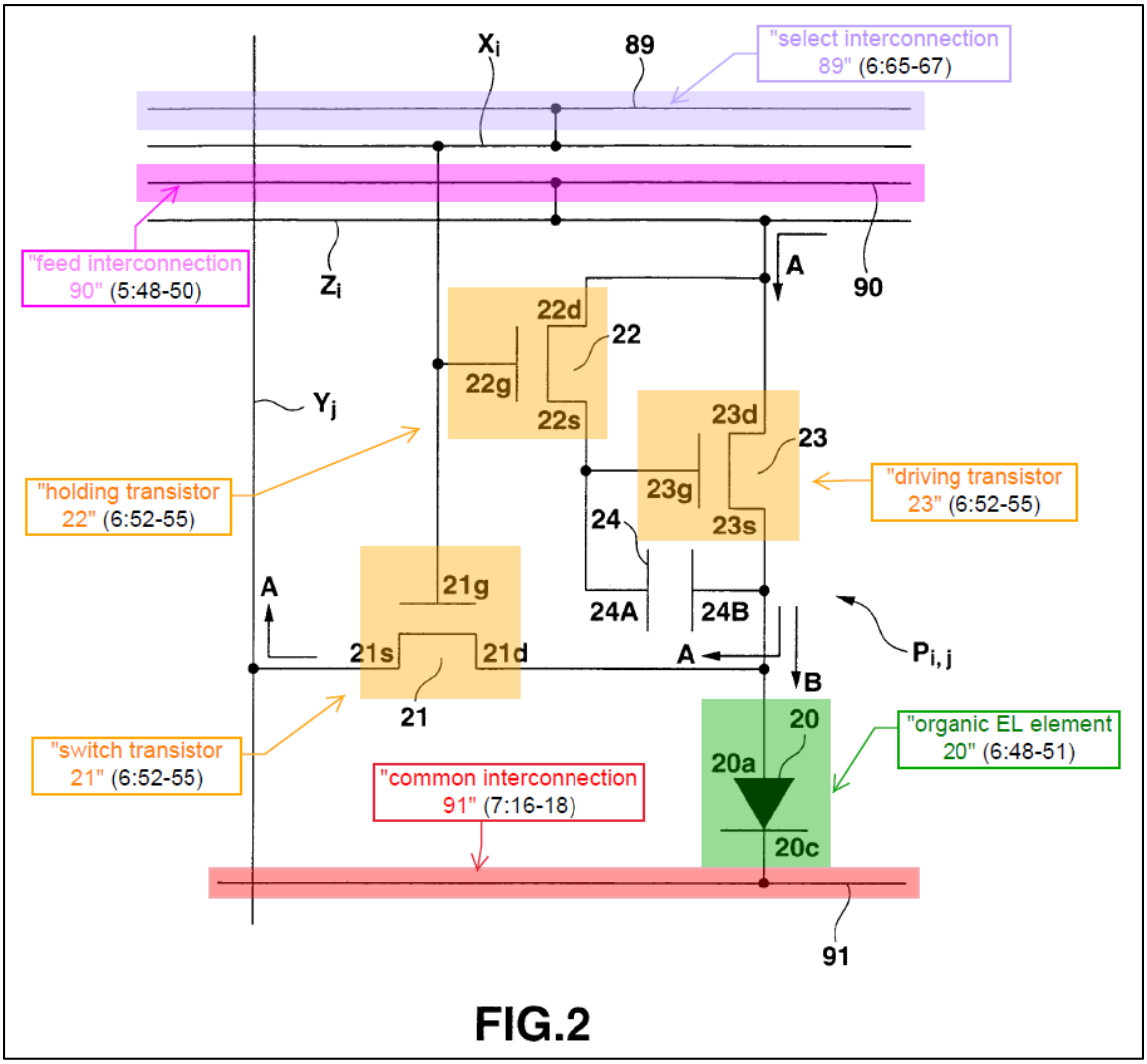


FIG.2

The ’338 patent explains that “switch transistor 21 functions to turn on (selection period) and off (light emission period) [] the current between the signal line Yj and the source 23s of the driving transistor 23,” Ex. 1001, 17:26–37, as illustrated by arrows “A” in Figure 2, above, *id.*, 16:30–41. If the switching transistor is on, “no driving current flows to the organic EL element 20, and no light emission occurs.” *Id.*, 17:24–25. The “holding transistor 22 functions to . . . hold the voltage between the gate 23g and the source 23s of the [driving] transistor 23 in the light emission period.” *Id.*, 17:29–37. Finally, the “driving transistor 23 functions to drive the organic EL element by supplying a current . . . to the organic EL element 20,” causing “the organic EL element [to] emit[] light.” *Id.* (with that “driving current” illustrated by arrow “B” in Figure 2, above, *id.*, 17:10–15); Ex. 1018, ¶¶ [0065]–[0066].

C. Prosecution History

As originally filed, claim 1 of the ’338 patent’s application contained only elements [a]–[e] listed above, and did not require the three-transistor pixel circuit (element [f]), i.e., a “driving transistor,” “holding transistor,” and “switch transistor.” Ex. 1002, 817 (September 26, 2005 originally filed claims). The Examiner rejected this original claim as anticipated by Yamazaki, noting that Yamazaki disclosed every limitation of the claim including the “plurality of interconnections which are formed to project to a surface of the transistor array substrate.” *Id.*, 446 (October 23, 2007

Non-Final Rejection) (citing "auxiliary electrode 621" and "auxiliary electrode 721" of Yamazaki as teaching the claimed "plurality of interconnections."). The Examiner stated, however, that originally filed dependent claim 2 (requiring that the "plurality of transistors includes a driving transistor . . . a switch transistor . . . and a holding transistor") would "be allowable if rewritten in independent form." *Id.*, 448, 817.

In response to this initial Office Action, the applicants amended claim 1 "to incorporate the subject matter of claim 2 [i.e. the three-transistor pixel circuit]," *id.*, 436 (February 25, 2008 Remarks), and the Examiner issued a Notice of Allowance for all pending claims, *id.*, 333 (May 30, 2008 Notice of Allowance).

The applicants never identified Shirasaki during prosecution. Two months after the issuance of the Notice of Allowance and the close of prosecution, the applicants submitted an Information Disclosure Statement identifying another application that listed Tomoyuki Shirasaki as the lead inventor—U.S. Patent Publication No. 2004/0165003 ("Shirasaki II") (Ex. 1007)—as well as its Japanese counterpart (JP 2004-258172) (Ex. 1008). *Id.*, 32–36 (August 5, 2008 IDS).

Because prosecution had closed, the applicants provided a statement under 37 C.F.R. § 1.97(e) representing that Shirasaki II was not "known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this Information Disclosure Statement," *id.*, even though Shirasaki II had been published

nearly four years earlier and Tomoyuki Shirasaki was also the lead named inventor of the '338 patent. The applicants also did not indicate in the IDS that Shirasaki II disclosed the same three-transistor pixel circuit as the '338 patent. *Compare* Ex. 1001, Fig. 2, *with* Ex. 1007, Fig. 1, Fig. 3.

After the applicants paid the issue fee on August 29, 2008, Ex. 1002, 31, the Examiner initialed the IDS on September 19, 2008, *id.*, 30, and the '338 patent issued on November 4, 2008.

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art ("POSA") of the '338 patent at the time of the alleged invention would have had a relevant technical degree in electrical engineering, computer engineering, physics, or the like, and 2–3 years of experience in active matrix display design and/or manufacturing. Ex. 1018, ¶¶ [0073]–[0074].

VI. CLAIM CONSTRUCTION

In IPR proceedings, claims are now construed "in accordance with their ordinary and customary meaning." 37 C.F.R. § 42.100(b); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). Petitioner discusses the meaning of certain claim limitations below.

A. "transistor array substrate" (claim 1)

The '338 patent describes the "transistor array substrate" as the layered structure on which the pixel electrodes are formed. The "transistor array substrate 50" is depicted in orange in annotated Figure 6 of the '338 patent below:

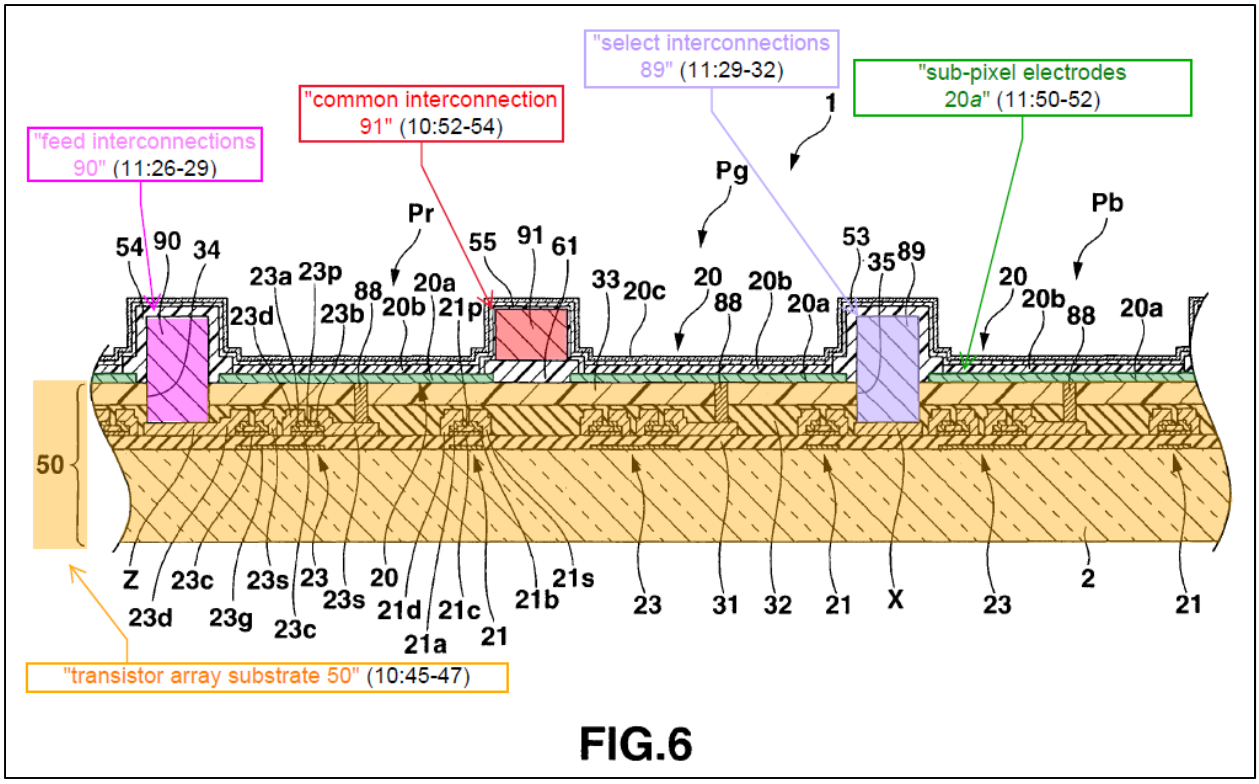


FIG.6

As Figure 6 demonstrates, the "transistor array substrate" includes all of the layers beneath the pixel electrodes, including the insulating substrate (element 2 in Figure 6), the gate insulating film (element 31 in Figure 6) and any additional planarization or other insulating layers above the transistor array and below the pixel electrodes (in Figure 6, protective insulating film 32 and planarization film 33). Ex. 1018, ¶¶ [0079]–[0081] (citing Ex. 1015, 8:38–58).

The '338 patent's specification describes the "transistor array substrate" as including all of the layers beneath the pixel electrodes, from the bottommost "insulating substrate" through the topmost insulating layer on whose surface the pixel electrodes are formed (in Figure 6, the planarization film 33), Ex. 1018, ¶ [0077]:

> The plurality of sub-pixel electrodes 20a are arrayed in a matrix on the upper surface of the planarization film 33, ***i.e., on the surface of the transistor array substrate 50***. The sub-pixel electrodes 20a are formed . . . by patterning a transparent conductive film formed on the entire surface of the planarization film 33.

Ex. 1001, 11:50–55 (emphasis added); *see also id.*, 10:48–51. *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1334 (Fed. Cir. 2009) ("the specification's use of 'i.e.' signals an intent to define the word to which it refers") (emphasis added).

Accordingly, this term should be interpreted as covering a layered structure including a bottom insulating substrate through a topmost insulating layer on whose surface the pixel electrodes are formed. Ex. 1018, ¶ [0082].

B. "a plurality of interconnections which are formed to project from a surface of the transistor array substrate" (claim 1)

Claim 1 refers to "a plurality of interconnections which are formed to project from a surface of the transistor array substrate." As noted above, the '338 patent defines the "surface of the transistor array substrate" as the upper surface of the topmost layer of the transistor array substrate, on which pixel electrodes are formed. Ex. 1001, 11:50–52, 10:48–51; Ex. 1018, ¶ [0083].

As to the meaning of "project from" a surface of the transistor array substrate, the '338 patent provides several examples. The specification describes how "common interconnection 91 is . . . formed to . . . project upward from the surface of the planarization film 33," Ex. 1001, 10:54–58, and "the select interconnection

89 and feed interconnection 90 project upward from the upper surface of the planarization film 33," *id.*, 11:36–41, as depicted in annotated Figure 6, Ex. 1018, ¶ [0083]:

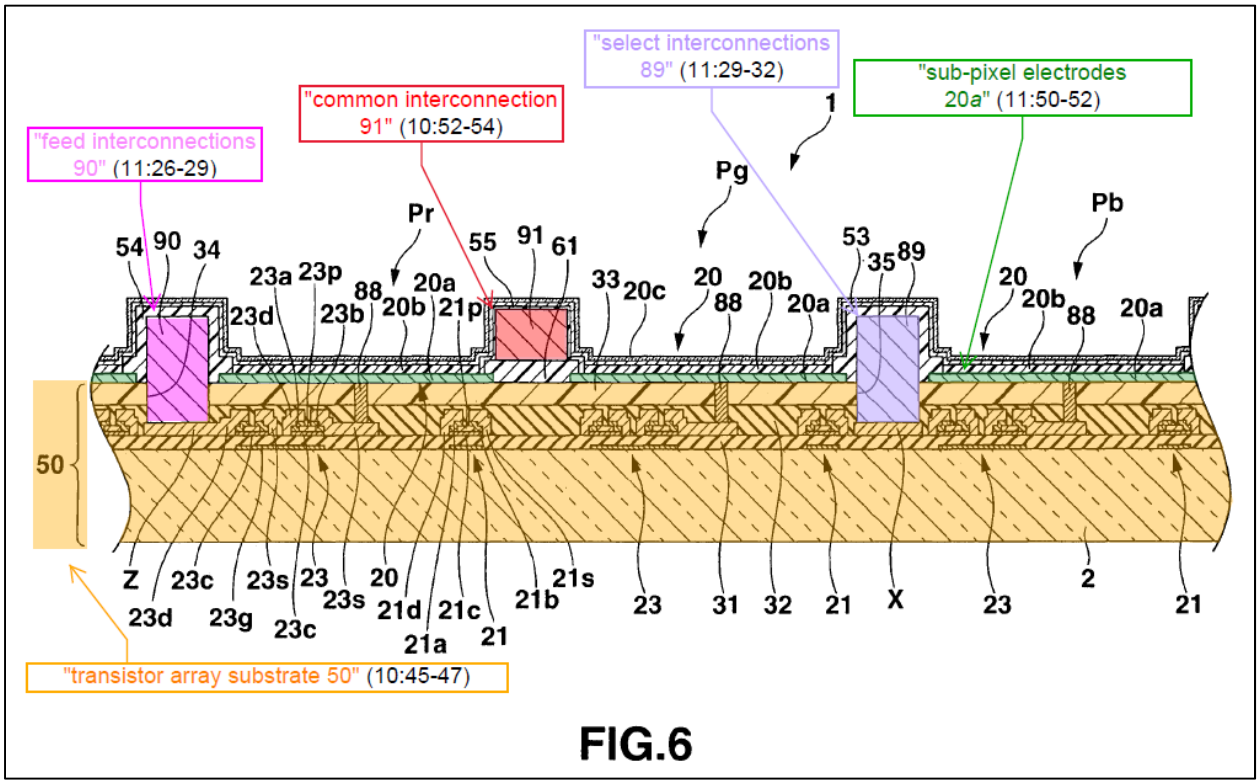


FIG.6

The '338 patent goes on to explain that each of "select interconnection 89, feed interconnection 90, and common interconnection 91 . . . are formed . . . to project respect to the surface of the transistor array substrate 50." Ex. 1001, 12:62–67; Ex. 1018, ¶ [0084].

Accordingly, this term should be interpreted to encompass a plurality of interconnections which are formed to extend above the upper surface of the topmost layer of the transistor array substrate (as in Figure 6, above). *Id.*

C. "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate" (claim 1)

As previously discussed, the "surface of the transistor array substrate" refers to the upper surface of the topmost insulating layer on which the pixel electrodes are formed. Ex. 1001, 11:50–52, 10:48–51. Petitioner submits that the proper interpretation of the claim limitation above is that the pixel electrodes: (1) are arrayed along the interconnections between the interconnections; and (2) are arrayed on the surface of the transistor array substrate. Ex. 1018, ¶ [0085].

This interpretation is supported by both the disclosure and claims of the '338 patent. The '338 patent states that "[t]he plurality of sub-pixel electrodes 20*a* are arrayed in a matrix on the upper surface of the planarization film 33, i.e., the upper surface of the transistor array substrate," Ex. 1001, 11:50–52, and that these sub-pixel electrodes are arrayed between the interconnections 89, 90, and 91, *id.*, 12:30–54, as depicted in annotated Figure 6, Ex. 1018, ¶ [0086]:

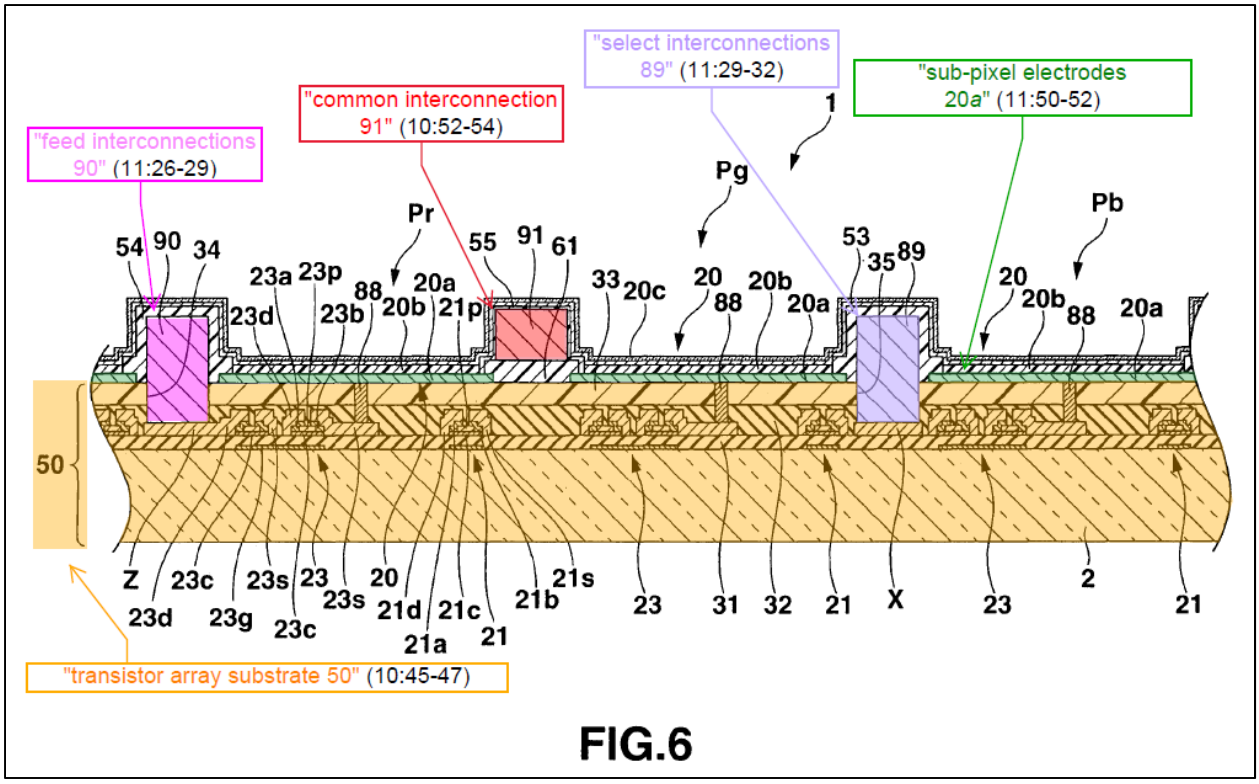


FIG.6

VII. OVERVIEW OF THE PRIOR ART

Both allegedly novel features of the ’338 patent were known in the prior art. That is, the prior art taught AMOLED display panels having (1) projecting “interconnections” between pixels and (2) a three-transistor pixel circuit structure that includes a “driving transistor,” “switch transistor,” and “holding transistor.” Both of these features were well known in the art.

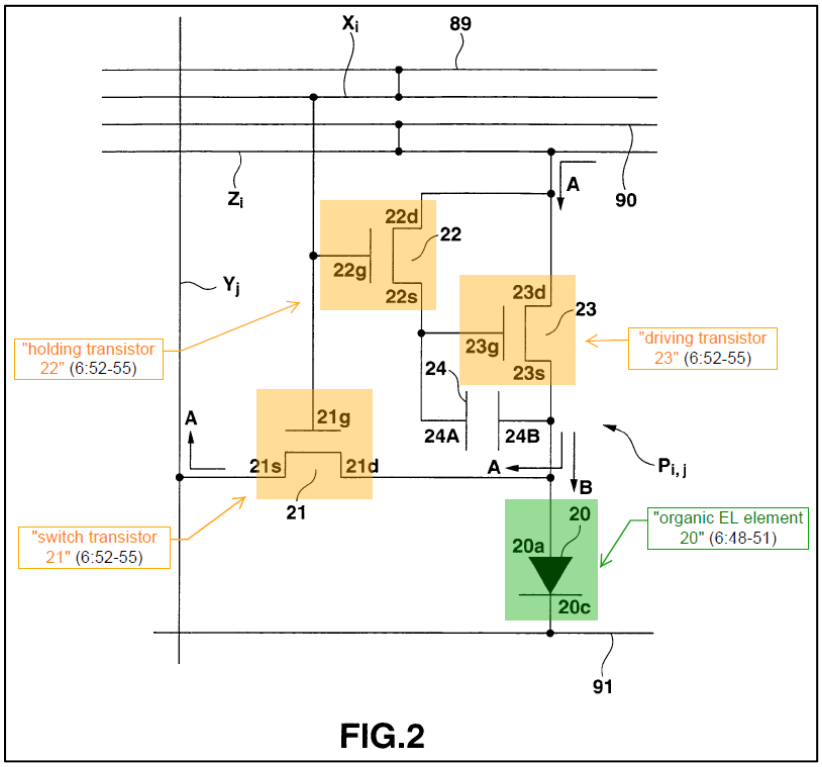
Regarding the first feature (the claimed “interconnections formed to project from a surface of the transistor array substrate”), it is clear from the prosecution history that this feature was not novel. For example, one of the patent’s specific examples of such a projecting interconnection is the “common interconnection 91,” which “reduce[s] the sheet resistance of the cathode electrode[s]” of “the organic EL

elements 20." Ex. 1003, 14:8–19. The Examiner explained that Yamazaki described such a common interconnection, citing to Yamazaki's "auxiliary electrode[s]" 621 and 721, Ex. 1002, 446 (October 23, 2007 Non-Final Rejection), which Yamazaki describes as "function[ing] to decrease an electric resistance value of the cathode" so that "the electrodes serving as a cathode . . . can be reduced in resistance as a whole, Ex. 1006, ¶ [0059]; Ex. 1018, ¶¶ [0036], [0069].

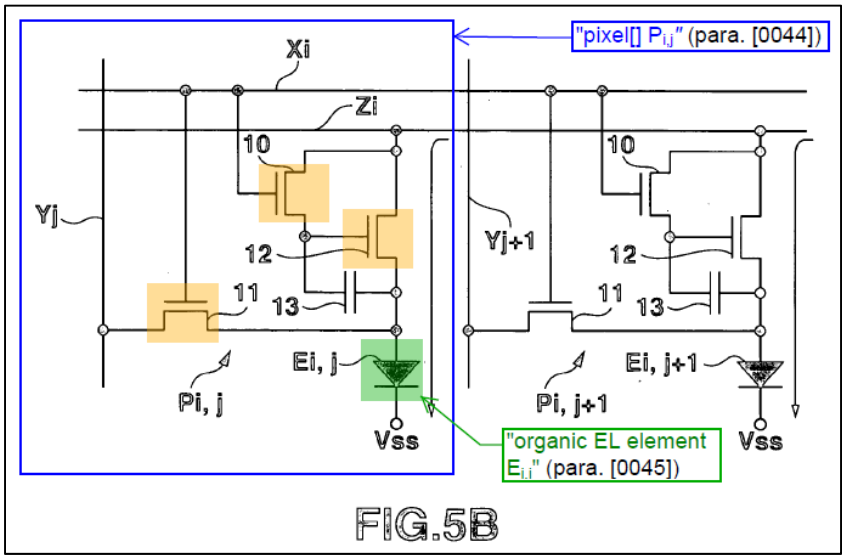
Other references also described OLED displays containing the type of projecting "interconnections" described and claimed in the '338 patent. Such references include: (1) U.S. Patent Application Publication No. 2002/0158835 ("Kobayashi"); and (2) International Publication No. WO 03/079441 ("Childs") relied on below as primary references for Grounds I and II, respectively. Ex. ¶¶ [0035]–[0040] (citing Exs. 1006, 1009–1011), [0087]–[0092] (citing Ex. 1003), [0096]–[0100] (citing Ex. 1005).

The second feature—the specific three-transistor structure found in each pixel of the claimed OLED display panel—was the feature that the Examiner believed was novel and that resulted in the allowance of the '338 patent. *Id.*, 448, 817 (October 23, 2007 Non-Final Rejection). But this feature, like the first, was not novel. Instead, it had been disclosed years earlier, including in a prior art reference by Tomoyuki Shirasaki, the first named inventor of the '338 patent. Ex. 1018, ¶¶ [0052]–[0053] (citing Ex. 1007), ¶¶ [0093]–[0095] (citing Ex. 1004). Indeed, that same three-

transistor pixel circuit is disclosed in diagrams of U.S. Patent Application Pub. No. 2004/0113873 ("Shirasaki") matching the diagrams later included in the '338 patent:



Ex. 1001 ('338 patent), Fig. 2 (annotated).



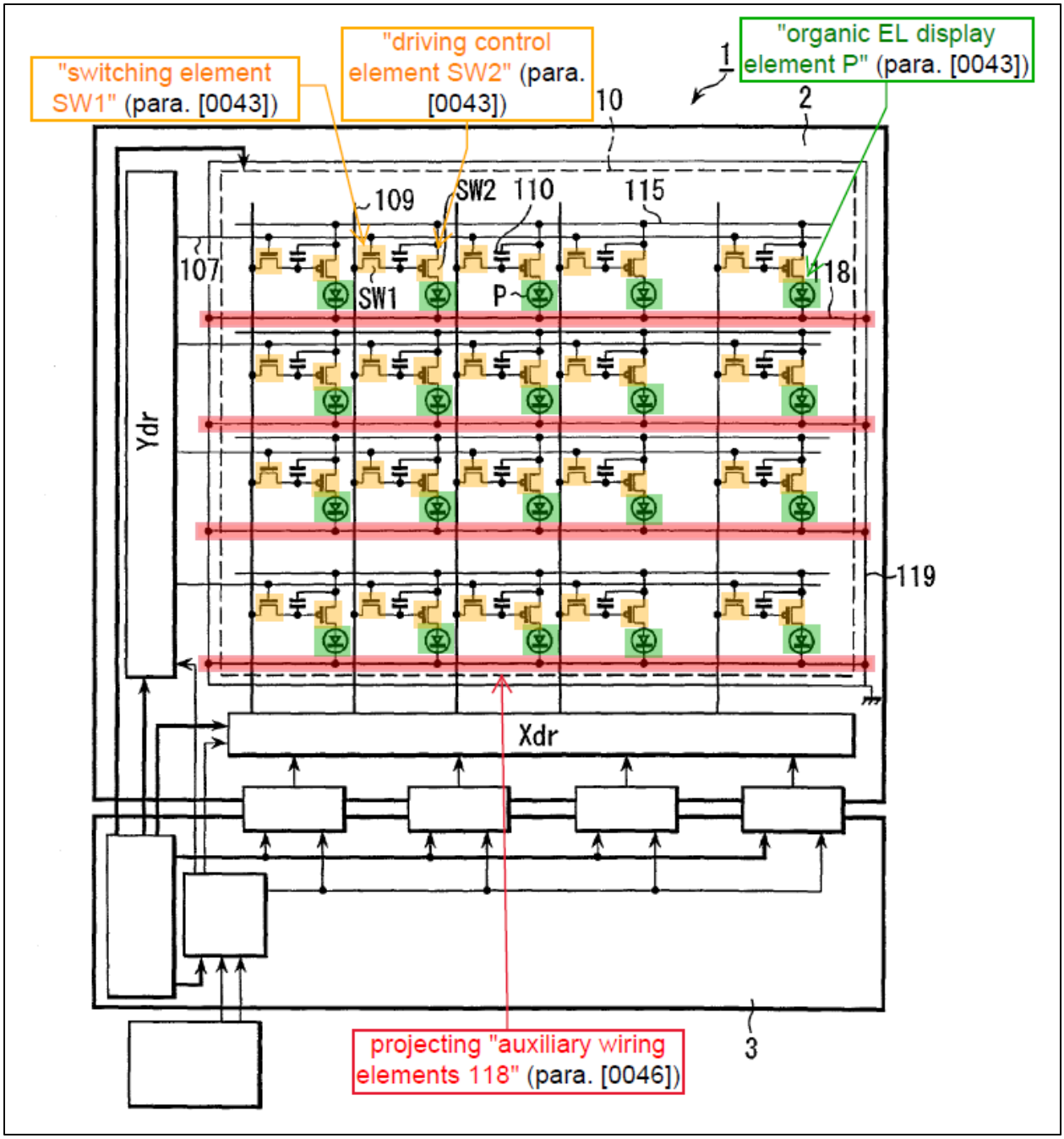
Ex. 1004 (Shirasaki), Fig. 5B (annotated).

A. Kobayashi (Ex. 1003)

Kobayashi is a U.S. Patent Application filed on April 19, 2002, and published on October 31, 2002, and thus is prior art under 35 U.S.C. §§ 102 (a), (b), and (e). Kobayashi was not cited or considered during prosecution.

Like the '338 patent, Kobayashi is directed to an AMOLED display panel. Kobayashi states that its "invention relates to a planar display device such as an organic electroluminescence (EL) display device"—and, "[i]n particular . . . to an active matrix type planar display device." Ex. 1003, ¶ [0001]. Kobayashi is particularly directed to the use of a projecting "auxiliary wiring element" that is "electrically connected to" the transparent cathode of the organic EL element, such that "the resistance of the entire [transparent cathode] can be lowered, and non-uniformity in display within the display screen can sufficiently be suppressed." *Id.*, ¶¶ [0061]–[0062]; Ex. 1018, ¶ [0087].

Annotated Figure 1 of Kobayashi displays "the structure of an organic EL display device," Ex. 1003, ¶ [0040]; Ex. 1018, ¶ [0088]:



"[O]rganic EL panel 2 comprises three kinds of display elements P, which respectively emit red, green, and blue light," and "are arranged in a matrix." Ex. 1003, ¶ [0041]. Each "organic EL display element P" is connected to two thin-film transistors (TFTs): a first "TFT functioning as a switching element SW1," and a

second "TFT functioning as a driving control element SW2." *Id.*, ¶ [0043]; Ex. 1018, ¶ [0089].

Notably, Kobayashi also includes projecting "auxiliary wiring elements 118," which are formed "in a lattice shape so as to surround . . . each display element P." *Id.*, ¶ [0046]; Ex. 1018, ¶ [0089]. Annotated Figure 7 displays an exemplary layered "structure of the organic EL display device 1" of Kobayashi, Ex. 1003, ¶ [0087]; Ex. 1018, ¶ [0090]:

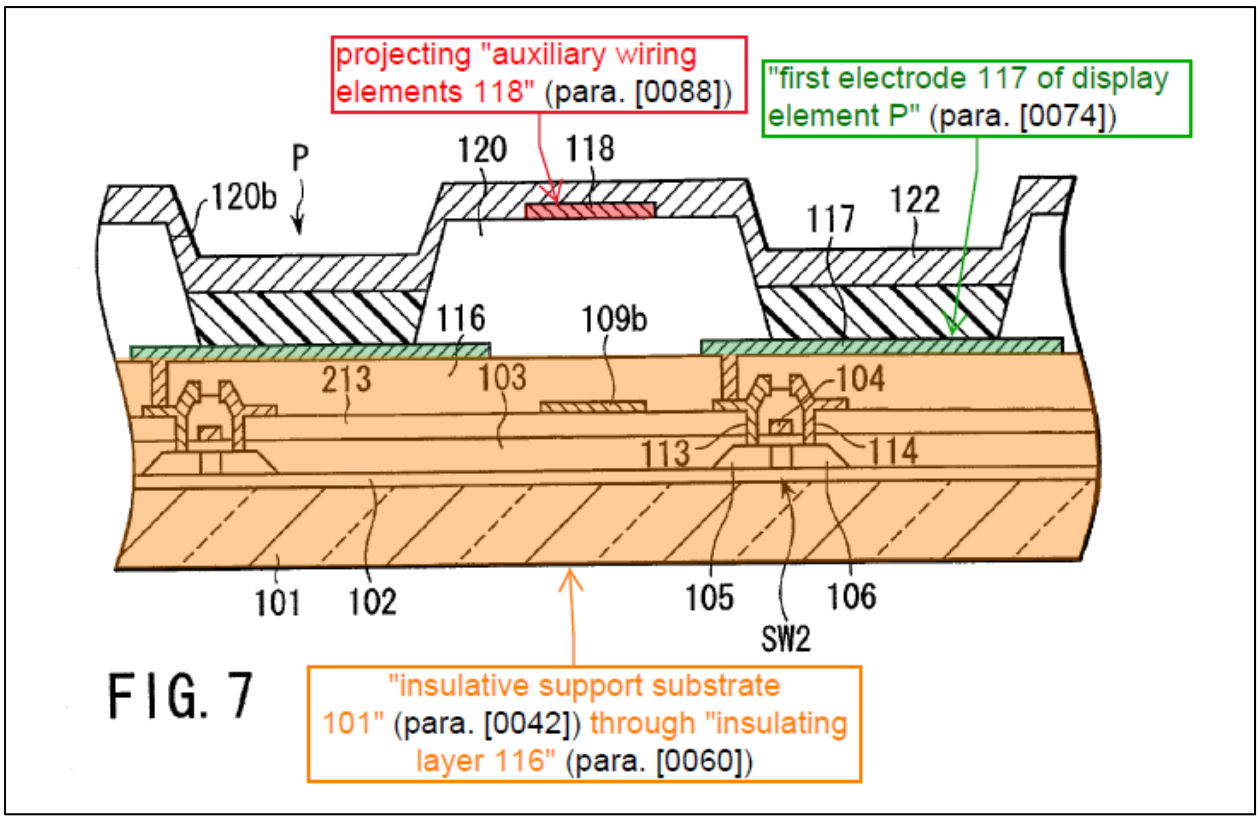


FIG. 7

TFTs SW1 and SW2 create "circuit[s] formed on the support substrate 101," Ex. 1003, ¶ [0084], a substrate made of "glass, etc.," *id.*, ¶ [0064]. An "insulating layer 116" (composed of a silicon nitride "film," *id.*, ¶ [0073]) is then formed "over the

TFTs . . . and [the] wiring under the insulating layer 116," *id.*, ¶ [0060]. The "first electrode 117 of display element P is [then] disposed on the insulating layer 116." *Id.*, ¶ [0074]; Ex. 1018, ¶ [0091].

In the structure of Figure 7, Kobayashi explains that "auxiliary wiring elements 118" are "electrically connected to the second electrode 122" and are "disposed in a lattice shape on partition walls 120 that electrically isolate the pixels in the display region" of the OLED device. Ex. 1003, ¶ [0088]. Kobayashi teaches that because auxiliary wiring element 118 has a lower resistance than electrode 122, *id.*, ¶ [0105], "[b]y electrically connecting the arranged auxiliary wiring elements 118 and second electrode 122, non-uniformity in voltage within the screen due to the resistance of the second electrode 122 can be suppressed . . . and the quality in display enhanced," *id.*, ¶ [0090]; Ex. 1018, ¶ [0092].

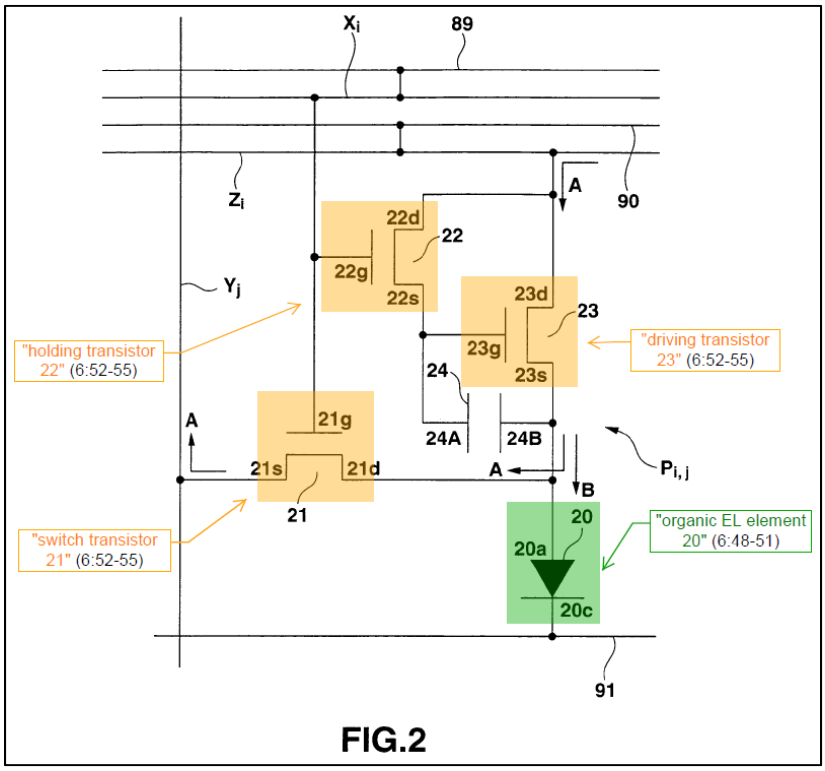
B. Shirasaki (Ex. 1004)

Shirasaki is a U.S. Patent Application published on June 17, 2004, more than one year before the September 26, 2005 filing date of the '338 patent. Shirasaki is thus prior art under 35 U.S.C. § 102(b). Shirasaki was not cited or considered during prosecution.

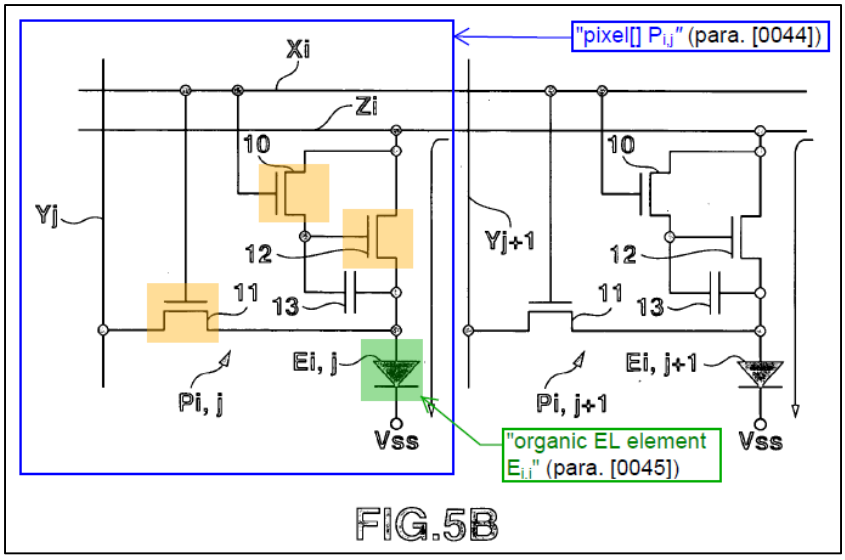
Shirasaki shares the same lead named inventor (Tomoyuki Shirasaki) and original assignee (Casio Computer Co.) as the '338 patent. Like the '338 patent, Shirasaki is directed to an AMOLED display panel. Ex. 1004, ¶¶ [0041] ("an active

matrix type light emitting panel"), [0043] ("a plurality of organic EL elements [] are arrayed in a matrix"); Ex. 1018, ¶ [0093].

Shirasaki's disclosure, like claim 1 of the '338 patent, is particularly directed to a three-transistor circuit structure for each pixel in its AMOLED display, including each of what the '338 patent would later term a "driving transistor," "switch transistor," and "holding transistor," as illustrated in the following comparison between Figure 2 of the '338 patent and Figure 5B of Shirasaki, Ex. 1018, ¶ [0094]:



Ex. 1001 ('338 patent), Fig. 2 (annotated).



Ex. 1004 (Shirasaki), Fig. 5B (annotated).

Shirasaki explains that the three-transistor pixel circuit of its invention improves on "conventional light emitting element display[s]" in which only "two transistors are formed in one pixel." Ex. 1004, ¶¶ [0003]–[0004], Fig. 11. Specifically, Shirasaki discloses that the three-transistor pixel circuit results in pixels that "stably display images with desired luminance in a display panel." *Id.*, ¶¶ [0011]–[0012], [0094]; Ex. 1018, ¶ [0095].

C. Childs (Ex. 1005)

Childs is an International Publication of a PCT application filed on February 21, 2003 in English, designating the United States. It published in English on September 25, 2003. Childs is therefore prior art under 35 U.S.C. §§ 102 (a), (b), and (e). Childs was not cited or considered during prosecution.

Like the '338 patent, Childs is directed to an AMOLED display panel. Ex. 1005, 1:5–7 (stating that Childs' "invention relates to active-matrix display devices,

particularly but not exclusively electroluminescent displays using light-emitting diodes of semiconducting conjugated polymer or other organic semiconductor materials."). Childs is particularly directed to "conductive barrier material 240 that is used as an interconnection" in such OLED devices. *Id.*, 6:25–29, 4:19–21. When "connected with a circuit element," *id.*, 2:29–3:5, the conductive barrier material reduces the resistance of that circuit element, "reduc[ing] voltage drops" along its length, *id.*, 3:17–25; Ex. 1018, ¶ [0096].

Annotated Figure 1 of Childs depicts its "pixel circuit configuration" with "drive" TFTs T1 and "addressing" TFTs T2, Ex. 1005, 7:1–17; Ex. 1018, ¶ [0097]:

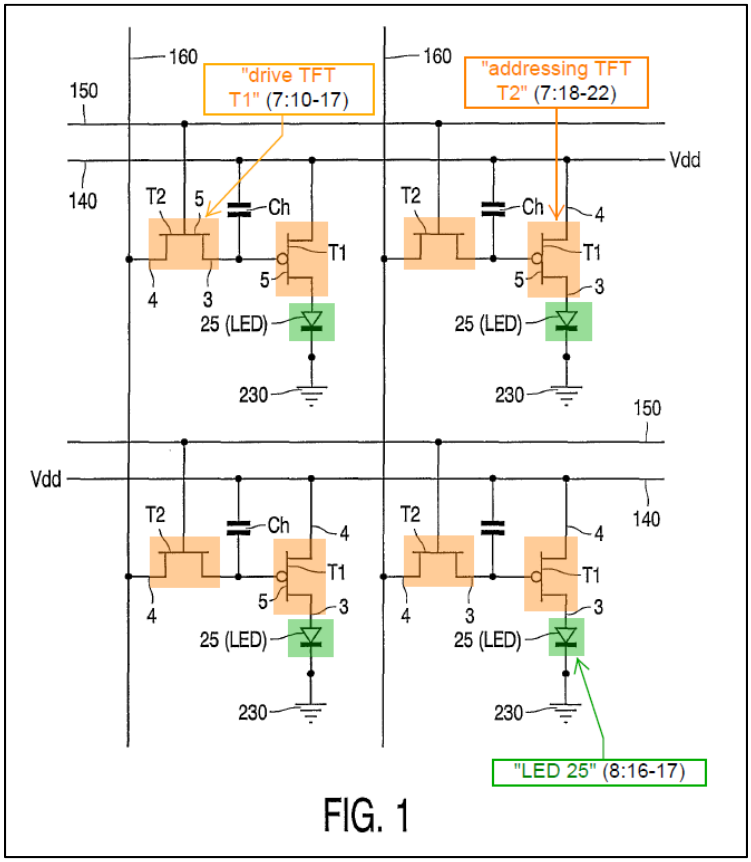


FIG. 1

Annotated "Figure 2 is a cross-sectional view of part of the pixel array and circuit substrate" of Childs' AMOLED display panel, Ex. 1005, 5:6–9, Ex. 1018, ¶ [0098]:

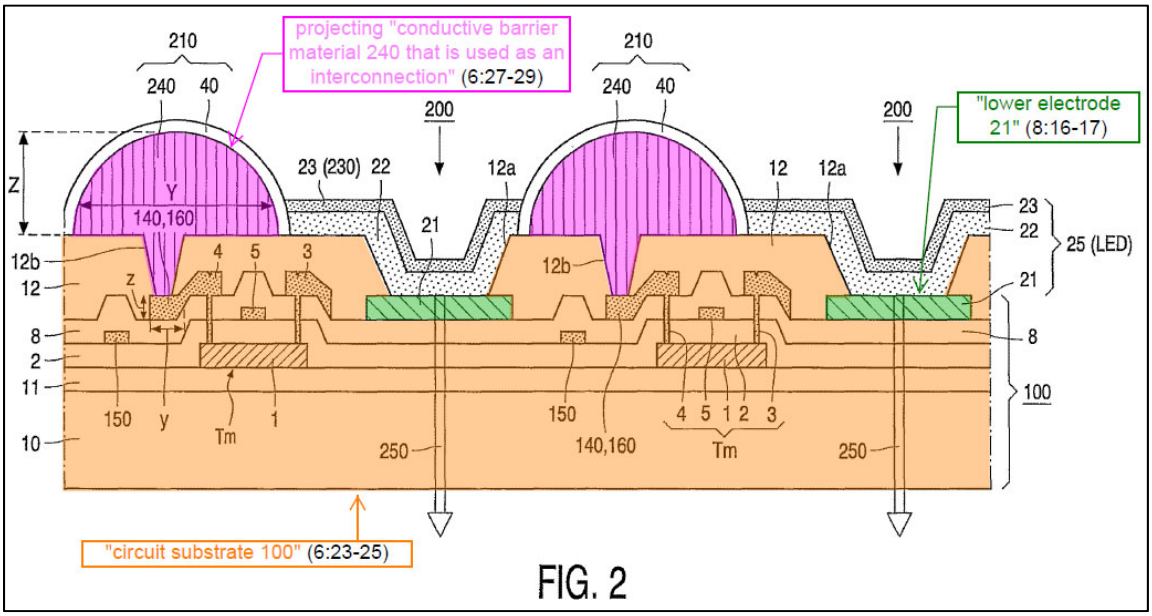


FIG. 2

Childs explains that the thin-film transistors of its pixel circuit are formed within "circuit substrate 100," which extends from "insulating glass base 10" to "planar insulating layer 12." Ex. 1005, 7:31–8:27, 14:30–32. Above the surface of planar insulating layer 12, "pixel barriers 210" are formed, acting as "dams" that "separate and prevent overflow of a polymer solution between the respective areas of the individual pixels 200" when "polymer layers 22" are being deposited. *Id.*, 8:28–9:17; Ex. 1018, ¶ [0099].

Childs teaches that pixel barriers 210 include "conductive barrier material 240 that is used as an interconnection." Ex. 1005, 6:25–29. These interconnections 240

are "preferably metal," *id.*, 10:6–8, and "are connected to and/or from one or more circuit elements of the circuit substrate 100," including "supply line 140" and/or "signal line 160," *id.*, 9:18–29. Because that metal has "very low resistivity," *id.*, 10:6–10, the resistance of a conductive line to which that interconnection is electrically connected "can be significantly reduced," *id.*, 10:25–27, 13:3–6, "reduc[ing] voltage drops along" that line, *id.*, 3:17–25; Ex. 1018, ¶ [0100].

VIII. APPLICATION OF PRIOR ART TO THE CHALLENGED CLAIMS

The framework for analyzing obviousness is set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1996), and the Petition analyzes the *Graham* factors below. Ground I details how claims 1–2, 5–6, and 9–11 were obvious based on the combination of Kobayashi and Shirasaki, and Ground II details how claims 1–3 and 5–13 were obvious based on the combination of Childs and Shirasaki. None of the prior art references or arguments in Grounds I–II was considered by the Examiner. The Fontecchio Declaration (Ex. 1018) was also not before the Examiner. Accordingly, none of the arguments raised in this Petition were previously presented to the USPTO. 35 U.S.C. § 325(d).

Further, the Grounds below are not duplicative or cumulative of one another. Ground I involves a primary reference (Kobayashi) that discloses one of the three types of "interconnections" recited in the challenged claims (the claimed "common

interconnection"), whereas Ground II involves a reference (Childs) that discloses the other two types of claimed "interconnections" ("feed" and "select interconnections").

A. Ground I: Claims 1–2, 5–6, and 9–11 Are Unpatentable Under 35 U.S.C. § 103 Over the Combination of Kobayashi and Shirasaki.

Claims 1–2, 5–6, and 9–11 are obvious over the combination of Kobayashi and Shirasaki.

Like the '338 patent, Kobayashi discloses an OLED display panel in which interconnections are connected to the OLED counter electrodes and project above the surface of the display panel's transistor array substrate (analogous to the '338 patent's "common interconnections"). Shirasaki, in turn, discloses the same three-transistor pixel circuit as used in the '338 patent's OLED display panel, and taught that this three-transistor pixel circuit improved performance over two-transistor pixel circuits. Accordingly, it would have been obvious to replace the two-transistor pixel circuits in Kobayashi's OLED display panel with Shirasaki's three-transistor pixel circuits to improve the OLED panel's functionality and display quality, and thus satisfy the challenged claims, as explained below. Ex. 1018, ¶¶ [0101]–[0102].

Because neither Kobayashi nor Shirasaki was before the Examiner, this Petition does not raise the same or substantially the same prior art or arguments previously considered by the USPTO. In fact, Shirasaki directly discloses the claim limitation that the Examiner believed was not found in the prior art and was responsible for allowance of the '338 patent: "wherein said plurality of transistors

for each pixel include a driving transistor . . . , a switch transistor . . . , and a holding transistor . . . .” Ex. 1002, 448, 817 (October 23, 2007 Non-Final Rejection).

1. Claim 1

1[preamble]: “A display panel comprising:”

To the extent the preamble is limiting, it is disclosed by Kobayashi. Kobayashi discloses “a planar display device such as an organic electroluminescent (EL) display,” and, “[i]n particular . . . an active matrix type planar display device.” Ex. 1003, ¶ [0001]; Ex. 1018, ¶ [0103].

1[a]: “a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain;”

The claimed “transistor array substrate” corresponds to the layered structure in Kobayashi extending from “insulating support substrate 101 of glass, etc.,” Ex. 1003, ¶ [0064], to “insulating layer 116” formed from “SiNx film,” *id.*, ¶ [0073], which creates a “plane” upon which “first electrode[s] 117” are formed, *id.*, ¶ [0080]. This layered structure is depicted in annotated Figure 7 of Kobayashi, Ex. 1018, ¶ [0106]:

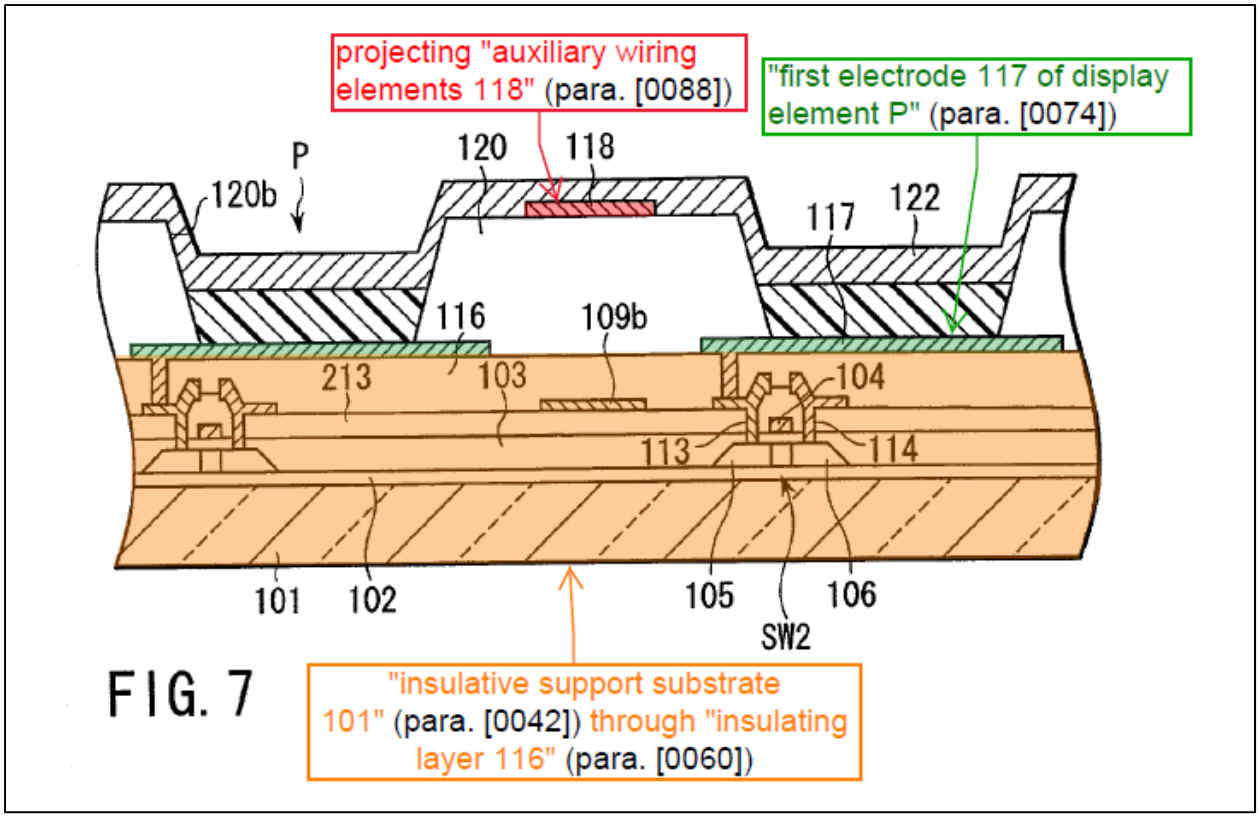


FIG. 7

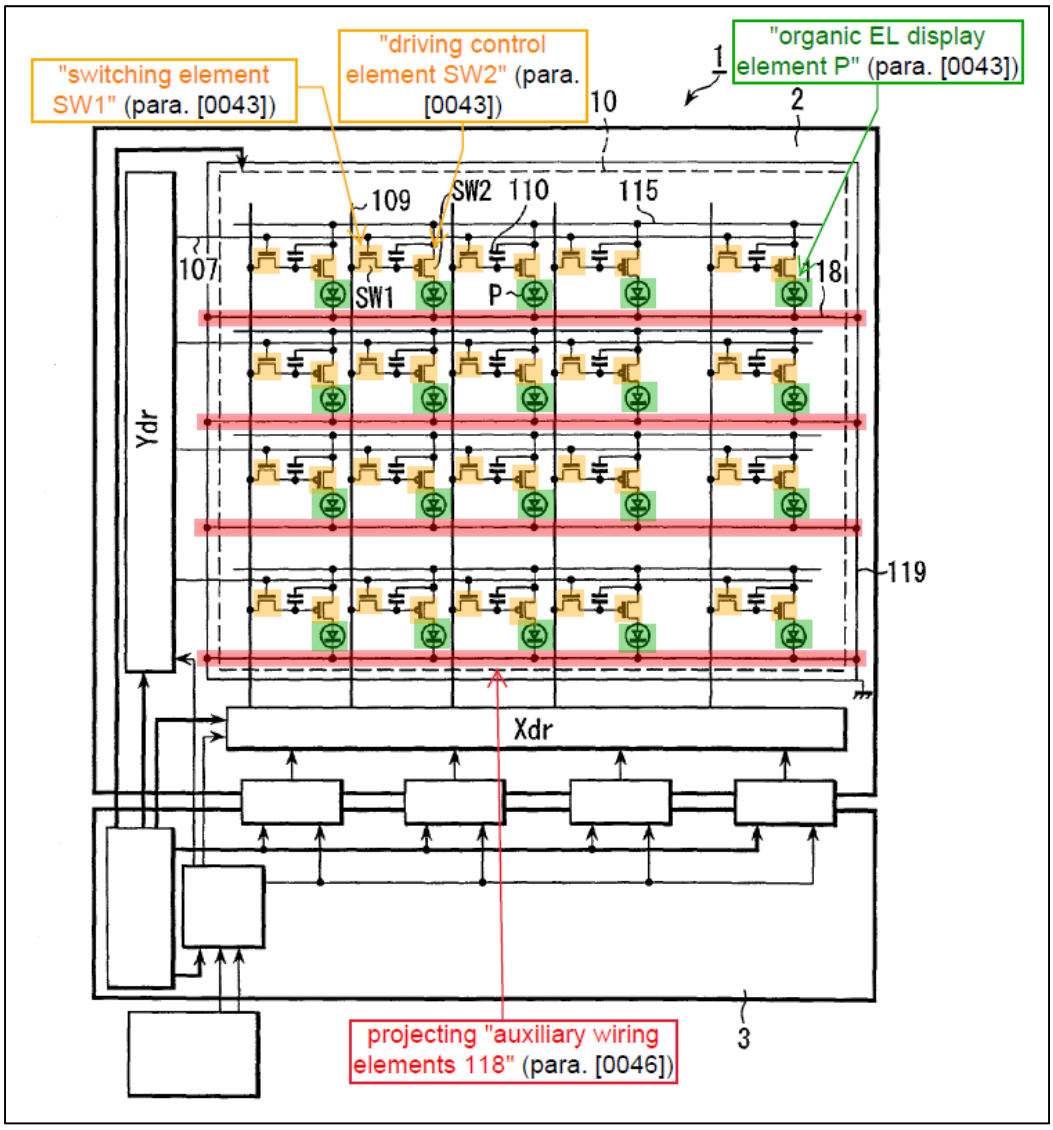
A POSA would have recognized that Kobayashi's layered structure from "support substrate 101" through "insulating layer 116" is a "transistor array substrate" as claimed in the '338 patent. Kobayashi's "support substrate 101" corresponds to the bottom insulating substrate 2 of the '338 patent's "transistor array substrate," and Kobayashi's "insulating layer 116" is the topmost insulating layer of the claimed substrate upon which Kobayashi's pixel electrodes 117 are formed. Ex. 1018, ¶ [0107].

Further, Kobayashi's layered structure extending from "support substrate 101" through "insulating layer 116" both (1) includes a plurality of pixels; and (2)

comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain:

"includes a plurality of pixels"

Kobayashi discloses that its "organic EL panel 2 comprises three kinds of display elements P" (i.e., pixels), "which respectively emit red, green, and blue light," and which "are arranged in a matrix" in "display region 10," as illustrated by annotated Figure 1 of Kobayashi, Ex. 1003, ¶ [0041]; Ex. 1018, ¶ [0109]:



Kobayashi discloses that display elements P (depicted above) are "pixels." *See, e.g.*, Ex. 1003, ¶¶ [0090]–[0091] ("auxiliary wiring elements 118 [are] arranged in a lattice shape . . . so as to surround the pixels of all display elements P"); Ex. 1018, ¶ [0110].

"comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain"

Kobayashi also discloses that its transistor array substrate comprises a plurality of transistors for each pixel. As illustrated in Figure 1 above, Kobayashi discloses that for each "organic EL display element P" (i.e., each pixel), "the organic EL panel 2 includes an n-type TFT functioning as a switching element SW1" and "a p-type TFT functioning as a driving control element SW2," Ex. 1003, ¶ [0043]. Kobayashi discloses that these thin-film transistors are located within the transistor array substrate, explaining that the "circuit [is] formed on the support substrate 101" (*id.*, ¶ [0084]) and "under the insulating layer 116" (*id.*, ¶ [0060]). Annotated Figure 7 of Kobayashi further shows TFT SW2 within the transistor array substrate (TFT SW1 is located on the same plane as SW2 but is not shown in this cross-sectional view), Ex. 1018, ¶¶ [0111]–[0113]:

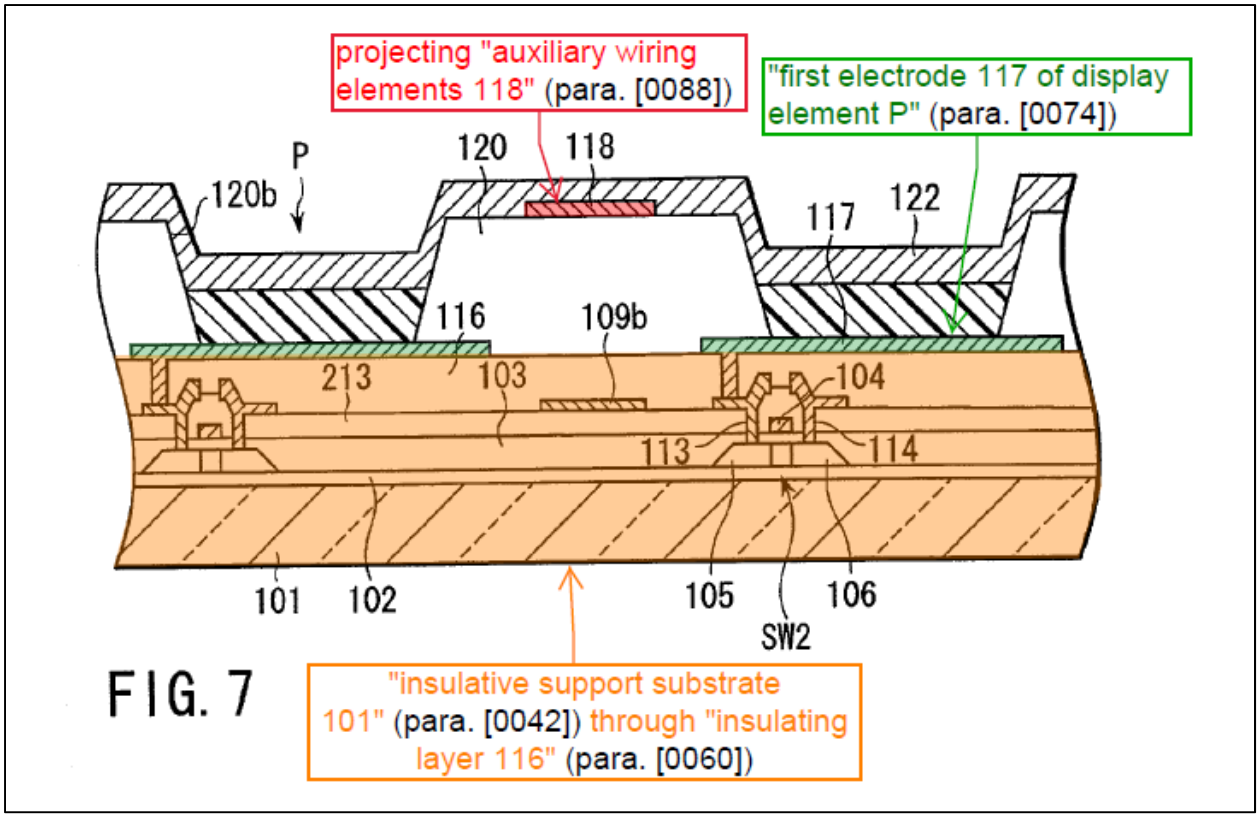


FIG. 7

Each of the p-type transistors SW2 comprises "a source region 105" (and connected "source electrode 113"), a "drain region 106" (and connected "drain electrode 114"), "a gate insulating film 103," and "a gate electrode 104," as illustrated above. Ex. 1003, ¶¶ [0066], [0070]. Similarly, each of the n-type transistors SW1 comprises "a source region 111" (and connected "source electrode 132"), "a drain region 112" (and connected "drain electrode 131"), "a gate insulating film 103," and "a gate electrode 108." *Id.*, ¶¶ [0068]–[0069], [0071]; Ex. 1018, ¶ [0114].

1[b]: "a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other;"

Kobayashi discloses this claim limitation. Specifically, Kobayashi discloses "auxiliary wiring elements 118 [that] are interconnected over the entire display region 10" and that project from the surface of "insulating layer 116" (i.e., the surface of the claimed transistor array substrate), Ex. 1003, ¶ [0088], as illustrated by annotated Figure 7 of Kobayashi, Ex. 1018, ¶ [0115]:

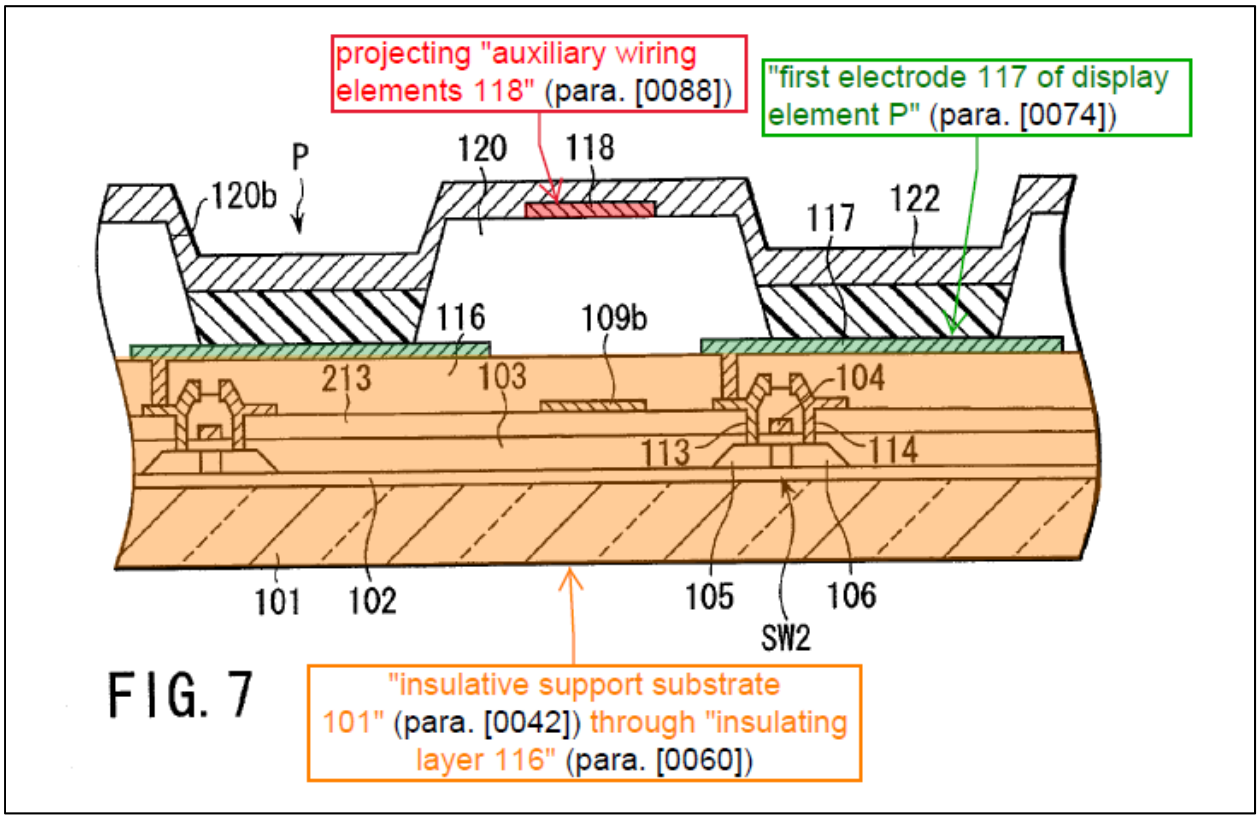


FIG. 7

These "auxiliary wiring elements 118" are "electrically connected to the second electrode 122," lowering the resistance of that electrode 122 to improve the uniform appearance of the display screen. Ex. 1003, ¶¶ [0062], [0083]. That is the same

purpose as the common interconnections in the ’338 patent, where “common interconnection 91 reduce[s] the sheet resistance of the cathode electrode.” Ex. 1001, 14:8–19; Ex. 1018, ¶ [0116].

Further, as shown in annotated Figure 7 of Kobayashi above, “auxiliary wiring elements 118” are formed on “partition walls 120” and extend above the surface of insulating layer 116, Ex. 1003, ¶ [0088], just as common interconnections 91 in the ’338 patent are formed on “insulating line 61” and extend above the surface of transistor array substrate 50, as depicted in annotated Figure 6, Ex. 1018, ¶ [0117]:

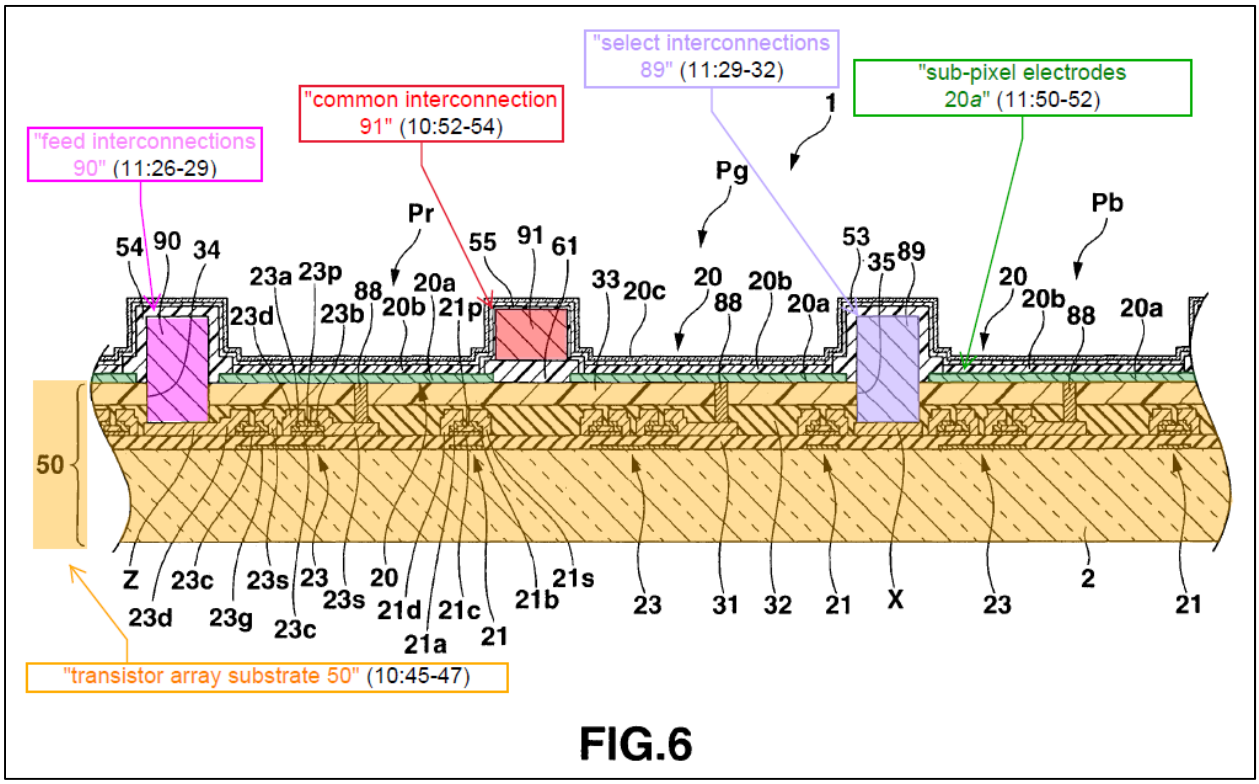
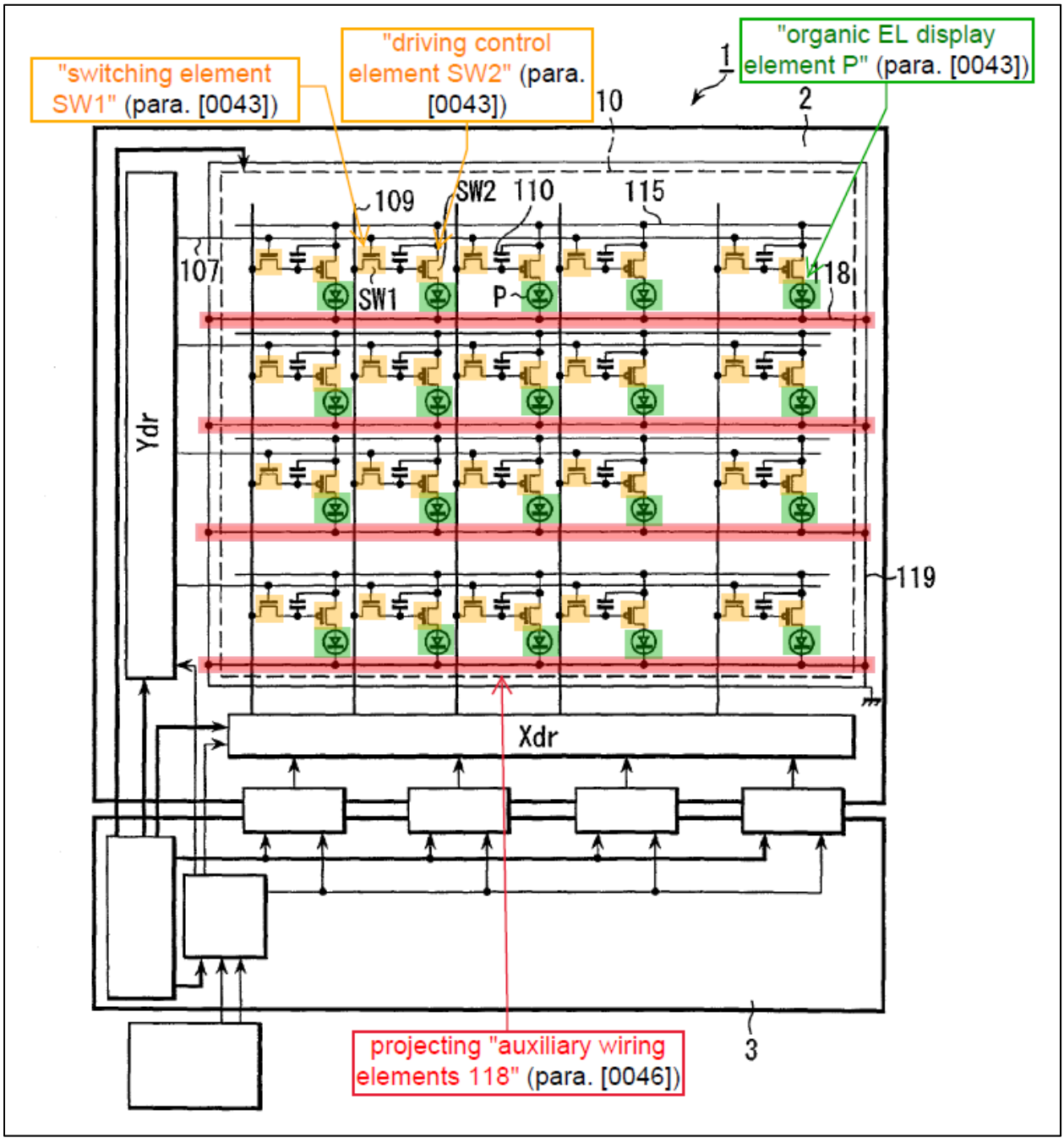


FIG.6

Kobayashi further discloses that its “auxiliary wiring elements 118” (the claimed plurality of interconnections) are arrayed in parallel to each other: “auxiliary

wiring elements 118 . . . are disposed in a lattice shape," Ex. 1003, ¶ [0088], as depicted in annotated Figure 1 of Kobayashi, Ex. 1018, ¶ [0118]:



1[c]: "a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along

the interconnections between the interconnections on the surface of the transistor array substrate;"

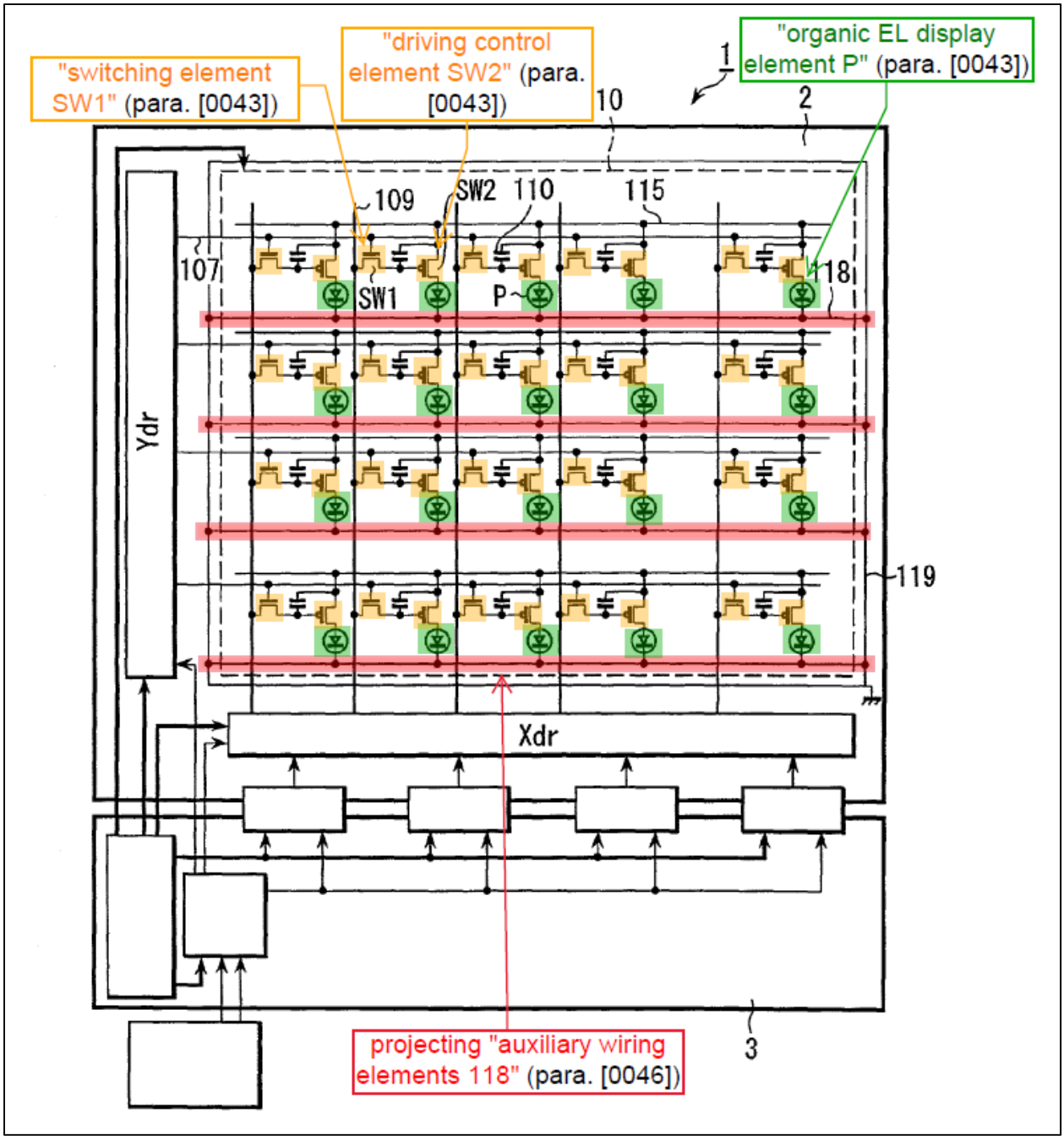
Kobayashi's "first electrodes 117" satisfy this claim limitation. Ex. 1003, ¶¶ [0057], [0092]; Ex. 1018, ¶ [0120].

"a plurality of pixel electrodes for the plurality of pixels, respectively"

Kobayashi discloses that each "organic EL display element P comprises a first electrode 117," Ex. 1003, ¶ [0044], which "functions as the anode of the organic EL display element," *id.*, ¶ [0051]; Ex. 1018, ¶ [0121].

"the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate"

Kobayashi discloses that its "auxiliary wiring elements 118" [the claimed "interconnections] "are formed in a lattice shape so as to surround the first electrode 117 of each display element P" [the claimed pixel electrodes], Ex. 1003, ¶ [0046]—in other words, to "surround the pixels of all display elements P," *id.*, ¶ [0090], as depicted in annotated Figure 1 of Kobayashi; Ex. 1018, ¶ [0122]:



Furthermore, Kobayashi discloses that first electrodes 117 [the claimed pixel electrodes] are "disposed on" the surface of "the insulating layer 116" [the upper surface of the claimed transistor array substrate], Ex. 1003, ¶ [0074], as illustrated by annotated Figure 7 of Kobayashi; Ex. 1018, ¶ [0123]:

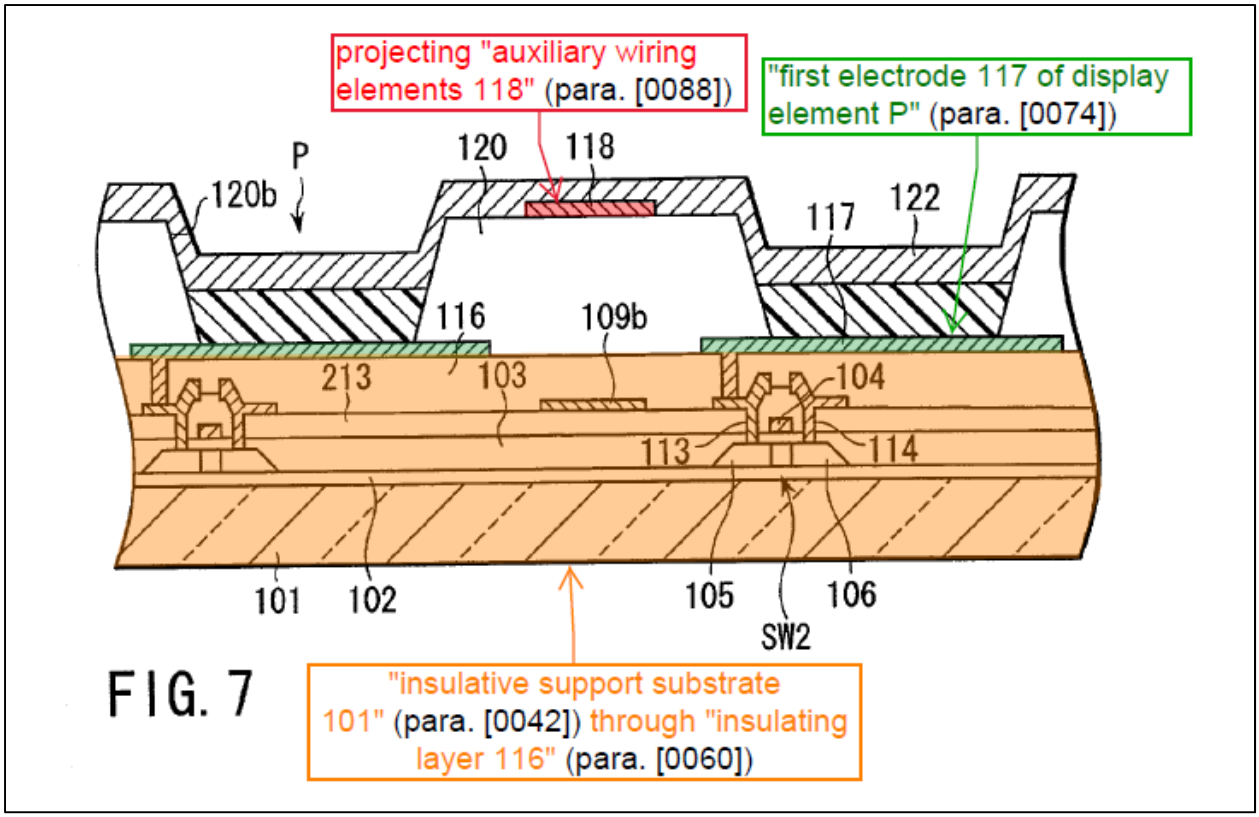


FIG. 7

1[d]: "a plurality of light-emitting layers formed on the pixel electrodes, respectively; and"

Kobayashi discloses "organic light-emission layers 121" that are "formed on"/ "disposed on" each "first electrode 117" in each "display element P." Ex. 1003, ¶¶ [0044], [0079]–[0080], [0092]; Ex. 1018, ¶ [0125].

1[e]: "a counter electrode which is stacked on the light-emitting layers,"

Kobayashi discloses a "second electrode 12" that "is provided commonly for all the display elements P," Ex. 1003, ¶ [0057], serves as the "cathode" "of the organic EL display element," *id.*, ¶ [0051], and is formed on organic light-emission layers 121 (see Figure 7, above), *id.*, ¶¶ [0044], [0080]; Ex. 1018, ¶ [0127]. Thus,

Kobayashi discloses a counter electrode (second electrode 12) which is stacked on the light-emitting layers (organic light-emission layers 121).

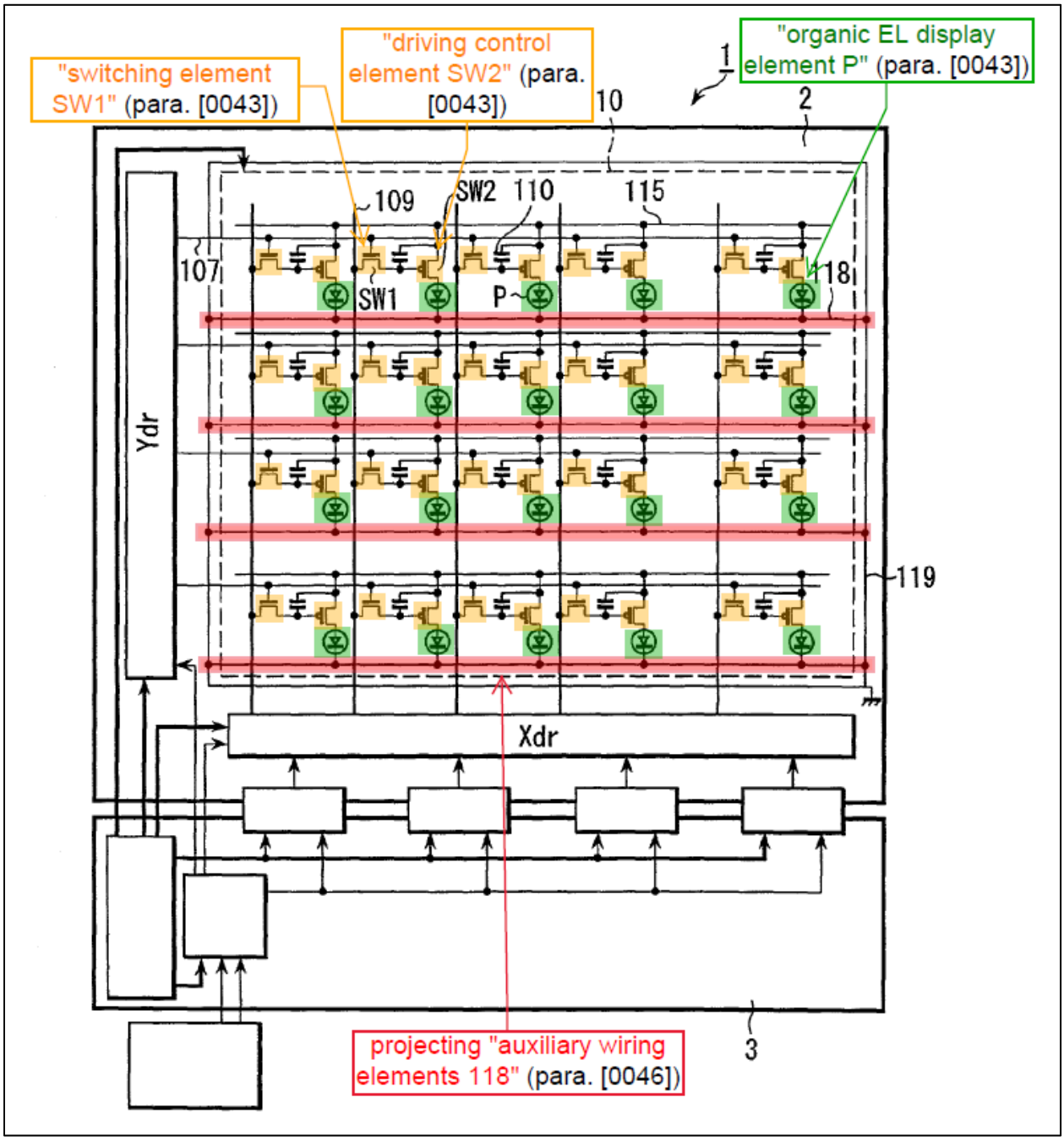
1[f]: "wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period."

Kobayashi discloses that each pixel includes the claimed "driving transistor" and "switch transistor," and it would have been obvious to further incorporate the claimed "holding transistor" in view of Shirasaki.

Specifically, Kobayashi discloses "driving control elements SW2," Ex. 1003, ¶ [0043], corresponding to the claimed "driving transistor, one of the source and the drain of which is connected to the pixel electrode." Kobayashi discloses that the source of this driving control element SW2 is connected to "the first electrode 117 of display element P" (the claimed pixel electrode). *Id.*, ¶ [0074]; Ex. 1018, ¶ [0131].

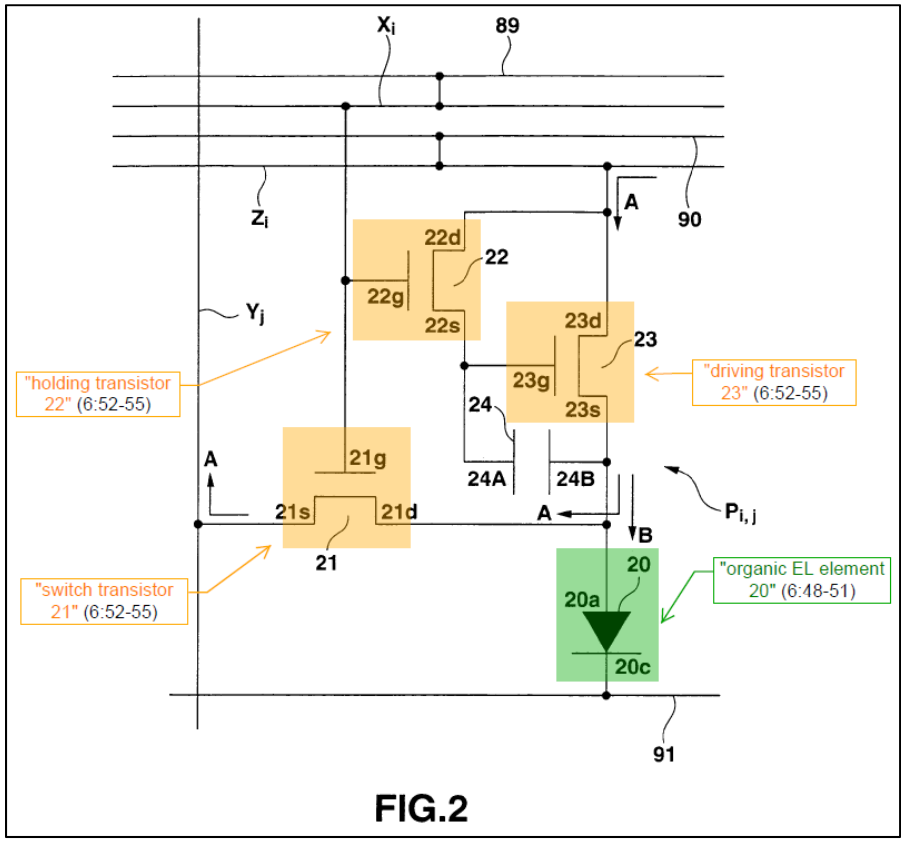
Kobayashi also discloses "switching elements SW1," Ex. 1003, ¶ [0043], corresponding to the claimed "switching transistor which makes a write current flow between the drain and the source of the driving transistor." The source of each switching element SW1 is connected to the gate of driving control element SW2 (thus controlling whether a current flows between the drain and source of driving

transistor SW2), as illustrated in annotated Figure 1 of Kobayashi; Ex. 1018, ¶ [0132]:

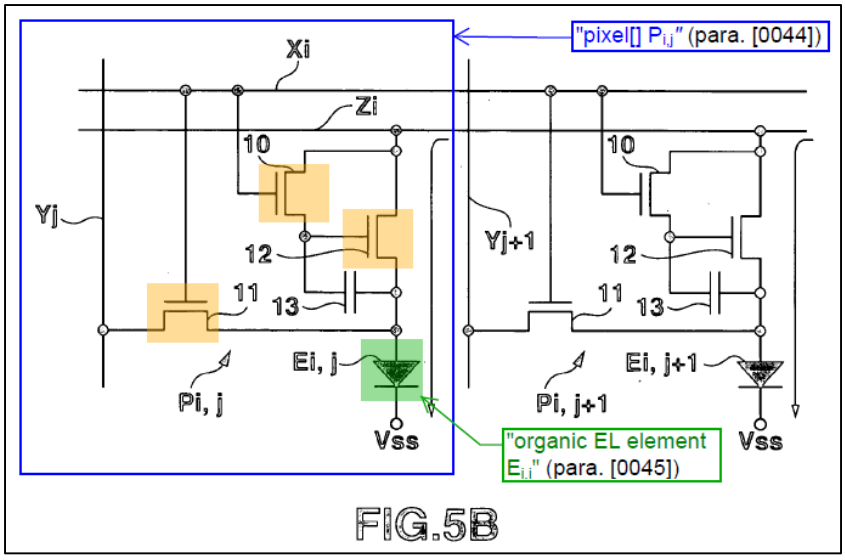


Kobayashi does not include a "holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period," as

claim 1 recites. However, adding this "holding transistor" limitation would have been obvious based on Shirasaki, which disclosed replacing a two-transistor-per-pixel circuit structure (as in Kobayashi) with a three-transistor-per-pixel circuit that includes each of the claimed "driving transistor," "switching transistor," and "holding transistor." In fact, Shirasaki's figures illustrate the same three-transistor pixel circuit that was later depicted in the '338 patent, Ex. 1018, ¶ [0133]–[0135]:



Ex. 1001 ('338 patent), Fig. 2 (annotated).



Ex. 1004 (Shirasaki), Fig. 5B (annotated).

Motivation to Combine:

Kobayashi and Shirasaki are both directed to improvements in AMOLED display panels and disclose TFT pixel circuits for use in AMOLED display panels. Shirasaki provides an express teaching, suggestion, or motivation to a POSA to replace Kobayashi's two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit. Specifically, Shirasaki notes that in a "conventional light emitting element display" in which "two transistors are formed in one pixel, Ex. 1004, ¶¶ [0003]–[0004]:

> The channel resistances of the transistors 103 and 104 depend upon the ambient temperature and change after a long-term operation. ***Therefore, it is difficult to display images with a desired luminance tone for long time periods.***
>
> . . .

> This varies the magnitudes of the drain-source currents of the transistors 104 in the individual pixels, resulting in variations in the display characteristics of the individual pixels in a single panel. ***As a consequence, no accurate tone control can be performed.*** Accordingly, variations in the characteristics of the transistor 104 of each pixel must fall within a range required to control the tone of each pixel. However, as the resolution of an EL element increases, ***it becomes more difficult to make the characteristics of the transistors 104 of the individual pixels uniform.***

Id., ¶ [0007] (emphasis added); Ex. 1018, ¶¶ [0136]–[0137].

By replacing a two-transistor pixel circuit (as in Kobayashi) with Shirasaki's three-transistor pixel circuit, Shirasaki explained that several advantages can be obtained:[4]

> In the display panel having the above [three-transistor] arrangement, the current memory circuit stores the current data corresponding to the current value of the memory current flowing during the selection period.

[4] While Kobayashi's pixel circuit includes a "capacitor 110 for holding a video signal voltage," Ex. 1003, ¶ [0043], this capacitor does not provide the same advantages as Shirasaki's "holding transistor"—the pixel circuits of both Shirasaki and the '338 patent still include a capacitor in addition to the "driving," "switch," and "holding" transistors, Ex. 1004, Figs. 1, 5A–B; Ex. 1001, Fig. 2; Ex. 1018, ¶ [0139].

> Accordingly, the display current having a current value substantially equal to the memory current can be supplied to the optical element. Current control is thus performed by the current values, not by voltage values. ***This suppresses the influence of variations in the voltage-current characteristic of the control system and allows the optical element to stably display images with desired luminance.***

Ex. 1004, ¶ [0018] (emphasis added); *see also id.*, ¶ [0011] ("[O]ne advantage of the present invention is that pixels stably display image with desired luminance in a display panel."); Ex. 1018, ¶¶ [0138]–[0139].[5]

For at least these reasons, the prior art provided a teaching, suggestion, or motivation to replace Kobayashi's two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit. This replacement would merely have been the "simple substitution of one known element [Shirasaki's three-transistor pixel circuit] for

[5] Shirasaki also explains why a POSA would have been motivated to use a three-transistor pixel circuit instead of a pixel circuit with "four or more transistors in one pixel." Ex. 1004, ¶ [0009]. Specifically, in comparison to a pixel circuit with four or more transistors, "the display area per pixel of a display panel is increased" and therefore "the apparent brightness improves accordingly," Ex. 1004, ¶¶ [0012], [0020], and the three-transistor circuit will have a comparatively "low voltage and consequently low power consumption driving," *id.*, ¶ [0019]; Ex. 1018, ¶ [0140].

another [Kobayashi's two-transistor pixel circuit]," and would have required no more than "the predictable use of prior art elements according to their established functions." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415–19 (2007); Ex. 1018, ¶ [0141].

Reasonable Expectation of Success:

Replacing Kobayashi's two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit would have been well within the skill of a POSA. As discussed above, Shirasaki expressly discloses that its three-transistor pixel circuit is meant to replace the two-transistor pixel circuit found in "conventional light emitting element display" devices (such as Kobayashi), and would have given a POSA a reasonable expectation of success in modifying Kobayashi in this manner. Ex. 1004, ¶¶ [0002]–[0008], [0013]–[0019]. And Kobayashi and Shirasaki each come from the same field of endeavor—active matrix organic light-emitting diode display panels featuring thin-film transistor arrays. Ex. 1003, ¶ [0002]; Ex. 1004, ¶¶ [0041], [0043]; Ex. 1018, ¶¶ [0142]–[0143].

Further, as disclosed above, Kobayashi expressly discloses that each of the transistors that make up its pixel circuits (and the wiring of that pixel circuit) are formed "under the insulating layer 116," with each "display element P . . . formed over" that insulating layer 116. Ex. 1003, ¶ [0060]; Ex. 1018, ¶ [0144]. And other contemporary prior art references similarly described separating the thin-film

transistors that make up the pixel circuit of an OLED device from the OLED elements themselves, via a planar insulating layer upon which the OLED elements are constructed. Ex. 1018, ¶¶ [0183]–[1085] (citing Exs. 1014, 1016, 1017).

Accordingly, a POSA would have recognized that the two-transistor pixel circuit in Kobayashi could be replaced with Shirasaki's three-transistor pixel circuit without altering any of the layers above the transistor array substrate in Kobayashi's layered OLED structure.[6] Kobayashi itself states that the light emission of its OLED elements is "irrespective of circuits such as TFTs" "under the insulating layer 116." Ex. 1003, ¶¶ [0060], [0004]. Making this obvious modification would have been no more than the "simple substitution of one known element [Shirasaki's three-transistor pixel circuit] for another [Kobayashi's two-transistor structure]," and would have required simply "the predictable use of prior art elements according to their established functions." *KSR*, 550 U.S. at 415–19; Ex. 1018, ¶ [0145].

[6] While making the change from Kobayashi's two-transistor pixel circuit to Shirasaki's three-transistor pixel circuit would have required changing the photomasks used to fabricate the TFT array and relocating the contact holes through Kobayashi's "insulating layer 116" that connect the TFT array to the OLED elements, these were routine and predictable manufacturing steps involved during the fabrication of every OLED display panel. Ex. 1018, ¶ [0146] (citing Ex. 1005).

2. Claim 2

"A panel according to claim 1, wherein said plurality of interconnections include at least one of a feed interconnection connected to the other of the source and the drain of at least one of the driving transistors, a select interconnection which selects at least one of the switch transistors, and a common interconnection connected to the counter electrode."

A POSA would have understood this claim to require that the plurality of interconnections include at least one of the three types of claimed interconnections ("feed," "select," or "common") (as opposed to requiring all three types of claimed interconnections, as recited by dependent claim 4). Ex. 1018, ¶ [0147]. And Kobayashi's interconnections constitute common interconnections connected to the counter electrode. As noted above, Kobayashi's "auxiliary wiring elements 118" are "electrically connected to the second electrode 122," lowering the resistance of that second electrode 122 to improve the uniform appearance of the display screen, Ex. 1003, ¶¶ [0062], [0083], just as the "common interconnection 91 reduce[s] the sheet resistance of the cathode electrode" in the '338 patent, Ex. 1001, 14:8–19; Ex. 1018, ¶ [0148].

3. Claim 5

"A panel according to claim 1, wherein said plurality of pixels include a red pixel, a green pixel, and a blue pixel."

Kobayashi discloses that its plurality of pixels include red pixels, green pixels, and blue pixels. Kobayashi states that its "organic EL panel 2 comprises three kinds

of display elements P, which respectively emit red, green, and blue light," Ex. 1003, ¶ [0041]; *see also id.*, ¶¶ [0044], [0056] (discussing the different colors of display elements/pixels P). Kobayashi further discloses that "organic light-emission materials corresponding to red (R), green (G), and blue (B) are successively jetted out by an ink-jet method," and thus that "organic light-emission layers 121 of the respective colors are selectively formed." *Id.*, ¶ [0079]; Ex. 1018, ¶ [0149].

4. Claim 6

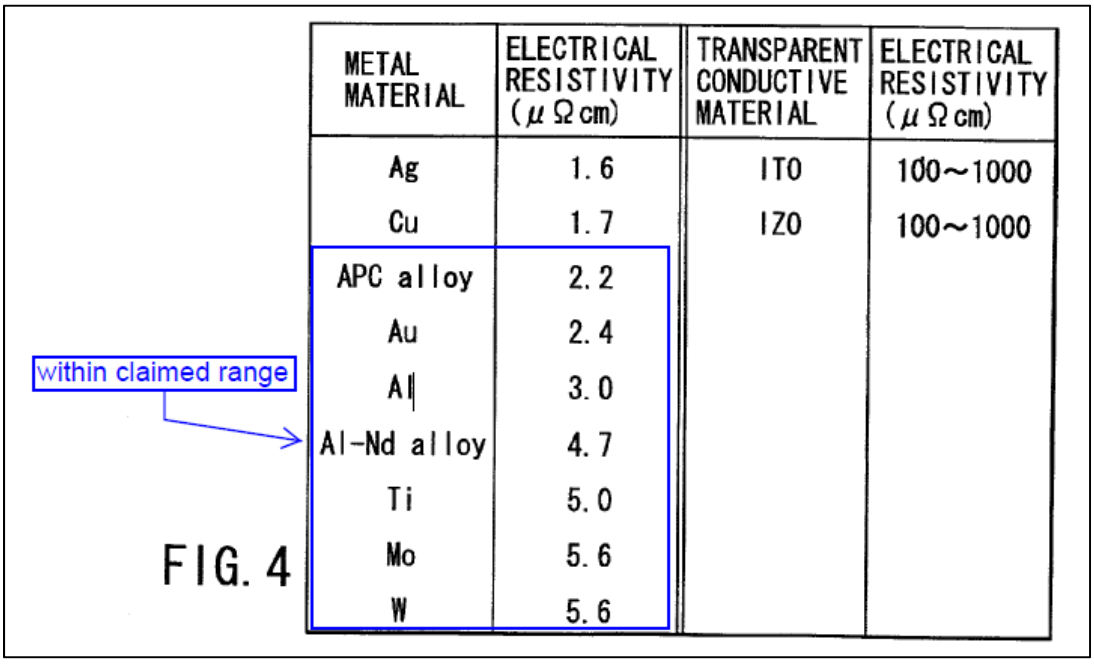
"A panel according to claim 5, wherein said plurality of pixels comprises a plurality of sets each including the red pixel, the green pixel, and the blue pixel arrayed in an arbitrary order."

A POSA would have recognized that Kobayashi's pixels comprise a plurality of sets each including the red pixel, the green pixel, and the blue pixel arrayed in an arbitrary order. As noted above, Kobayashi states that its "organic EL panel 2 comprises three kinds of display elements P, which respectively emit red, green, and blue light," Ex. 1003, ¶ [0041], and that "organic light-emission materials corresponding to red (R), green (G), and blue (B) are successively jetted out by an ink-jet method," and thus that "organic light-emission layers 121 of the respective colors are selectively formed," *id.*, ¶ [0079]; Ex. 1018, ¶¶ [0151]–[0152] (citing Ex. 1007).

5. Claim 9

"A panel according to claim 1, wherein at least one of the interconnections has a resistivity of 2.1 to 9.6 μΩcm."

Kobayashi teaches that "it is preferable, in particular, that the auxiliary wiring element" (the claimed interconnections) "be formed of a conductive material with a resistivity of $1x10^{-6}$ Ωcm to $6x10^{-6}$ Ωcm," Ex. 1003, ¶ [0049], and specifically provides an example in which the "resistivity of the auxiliary wiring element 118 . . . is about 3 μΩcm," *id.*, ¶ [0089]. Additionally, annotated Figure 4 of Kobayashi provides "the electrical resistivity (μΩcm) of typical metal materials chosen for the auxiliary wiring element 118," including a number of materials having resistivities in the claimed range, *id.*, ¶ [0049]; Ex. 1018, ¶ [0154]:



METAL MATERIAL	ELECTRICAL RESISTIVITY (μΩcm)	TRANSPARENT CONDUCTIVE MATERIAL	ELECTRICAL RESISTIVITY (μΩcm)
Ag	1.6	ITO	100~1000
Cu	1.7	IZO	100~1000
APC alloy	2.2		
Au	2.4		
Al	3.0		
Al-Nd alloy	4.7		
Ti	5.0		
Mo	5.6		
W	5.6		

FIG. 4

6. Claim 10

"A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer that is different from a layer forming the source and the drain of each of the transistors and a layer forming the gate of the transistors."

Kobayashi's "auxiliary wiring elements 118" (the claimed plurality of interconnections) are formed from "metal materials," Ex. 1003, ¶ [0049], whereas the source, drain, and gate of its transistors are formed from polysilicon, *id.*, ¶¶ [0065]–[0069]. And as illustrated in annotated Figure 7 of Kobayashi, the "auxiliary wiring elements 118" are formed from a conductive layer that is different than the layer forming the source and drain 105 and 106 of each of transistors SW2, or the layer forming the gate 104 of transistors SW2, each of which is buried under insulating layer 116, Ex. 1018, ¶ [0156]:

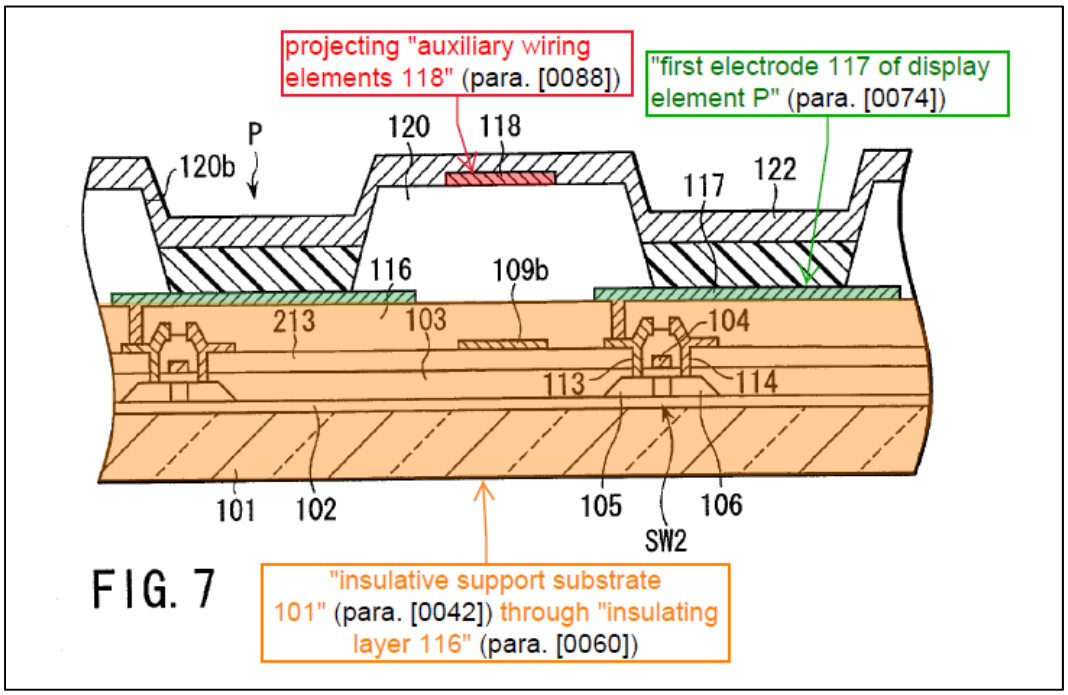


FIG. 7

7. Claim 11

"A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer different from a layer forming the pixel electrodes."

As illustrated in annotated Figure 7 of Kobayashi, Kobayashi's "auxiliary wiring elements 118" (the claimed plurality of interconnections) are formed in a conductive layer on top of insulating "partition wall[s] 120," which in turn are formed on top of the layer forming the "first electrode[s] 117" (the claimed pixel electrodes), Ex. 1003, ¶ [0092], Ex. 1018, ¶ [0158]:

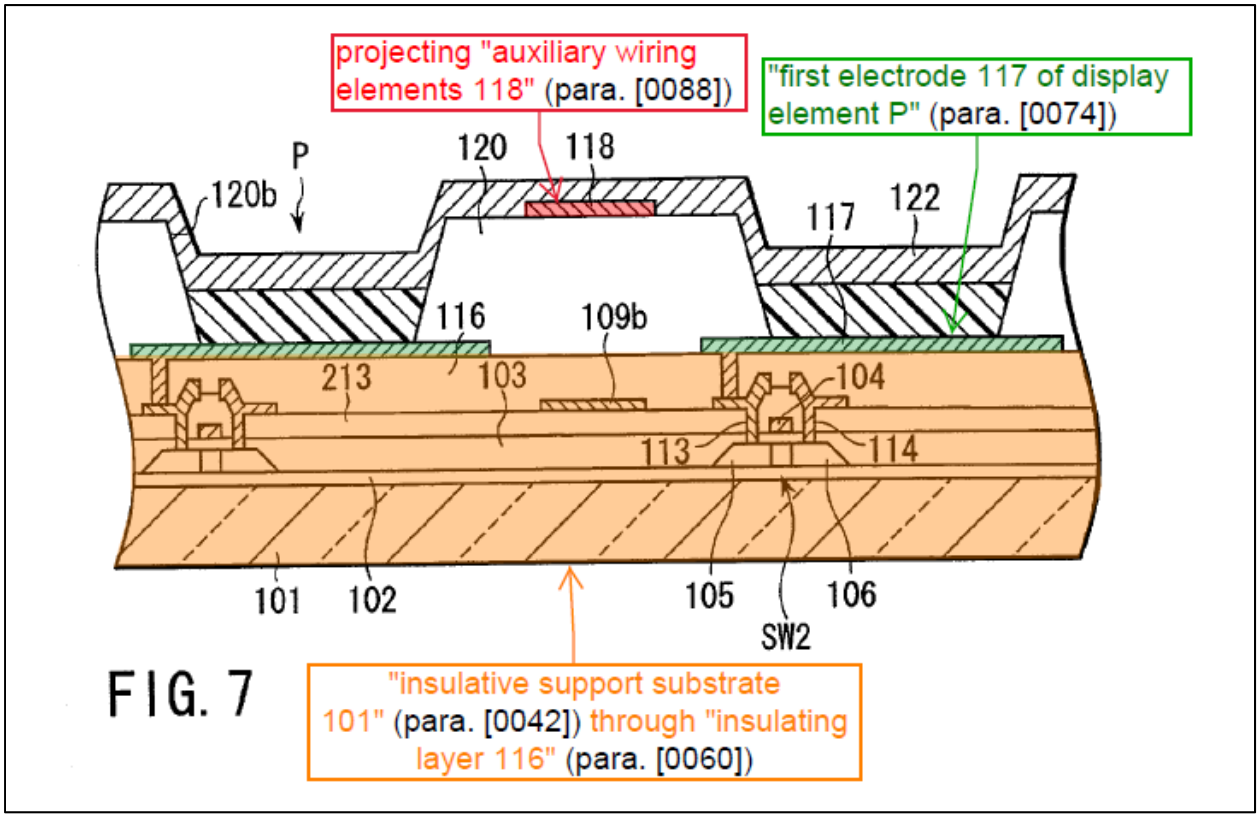


FIG. 7

B. Ground II: Claims 1–3 and 5–13 Are Unpatentable Under 35 U.S.C. § 103 Over the Combination of Childs and Shirasaki.

Claims 1–3 and 5–13 of the ’338 patent are obvious over the combination of Childs and Shirasaki.

Like the ’338 patent, Childs discloses an OLED display panel with interconnections connected to a supply line (analogous to the ’338 patent’s “feed interconnections”) and interconnections connected to an addressing line (analogous to the “select interconnections”), where both types of interconnections project above the surface of the display panel’s transistor array substrate. Shirasaki, in turn, discloses the same three-transistor circuit that is used in the pixels of the ’338 patent’s OLED panel. Accordingly, as explained below, it would have been obvious to replace the two-transistor pixel circuits in Childs’ OLED display panel with Shirasaki’s three-transistor pixel circuit to improve the functionality and display quality of that OLED display, and thus satisfy the challenged claims, as explained below.

Because neither Childs nor Shirasaki was before the Examiner, this Petition does not raise the same or substantially the same prior art or arguments previously considered by the USPTO. In fact, Shirasaki directly discloses the claim limitation that the Examiner believed was missing from the prior art and that resulted in the allowance of the ’338 patent: “wherein said plurality of transistors for each pixel

include a driving transistor . . . , a switch transistor . . . , and a holding transistor . . . ." Ex. 1002, 448, 817 (October 23, 2007 Non-Final Rejection).

1. Claim 1

1[preamble]: "A display panel comprising:"

To the extent the preamble is limiting, it is disclosed by Childs. Childs discloses an "active-matrix electroluminescent display (AMELD) device." Ex. 1005, 6:23–25; Ex. 1018, ¶ [0162].

1[a]: "a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain;"

Childs discloses the claimed transistor array substrate. Childs describes the layered structure of "circuit substrate 100," which extends from "insulating glass base 10" through "insulating layers" 11, 2 and 8 and "planar insulating layer 12." Ex. 1005, 6:23–25, 7:31–8:27, 14:30–32 ("the thin-film circuit substrate 100 with its upper planar insulating layer 12"). This layered structure of circuit substrate 100 is depicted in annotated Figure 2 of Childs, Ex. 1018, ¶ [0165]:

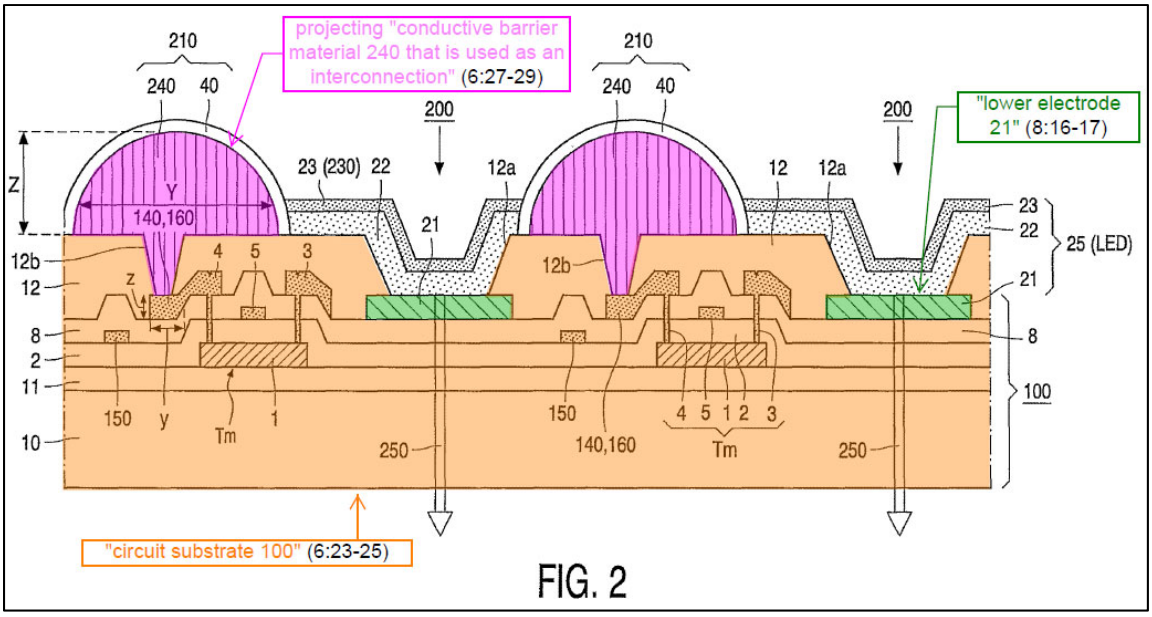


FIG. 2

A POSA would have recognized that the layered structure of Childs' "circuit substrate 100" (which extends from "insulating glass base 10" through "planar insulating layer 12") comprises a "transistor array substrate" as claimed in the '338 patent. Ex. 1018, ¶ [0166]. The layered structure of Childs' circuit substrate 100 both (1) includes a plurality of pixels; and (2) comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain:

"includes a plurality of pixels"

Childs discloses that its "active-matrix electroluminescent display (AMELD) device . . . comprises an array of pixels 200 on a circuit substrate 100," with "[p]hysical barriers 210 . . . between at least some of the neighbouring pixels," Ex. 1005, 6:23–27, as depicted in annotated Figure 2 of Childs, Ex. 1018, ¶ [0168]:

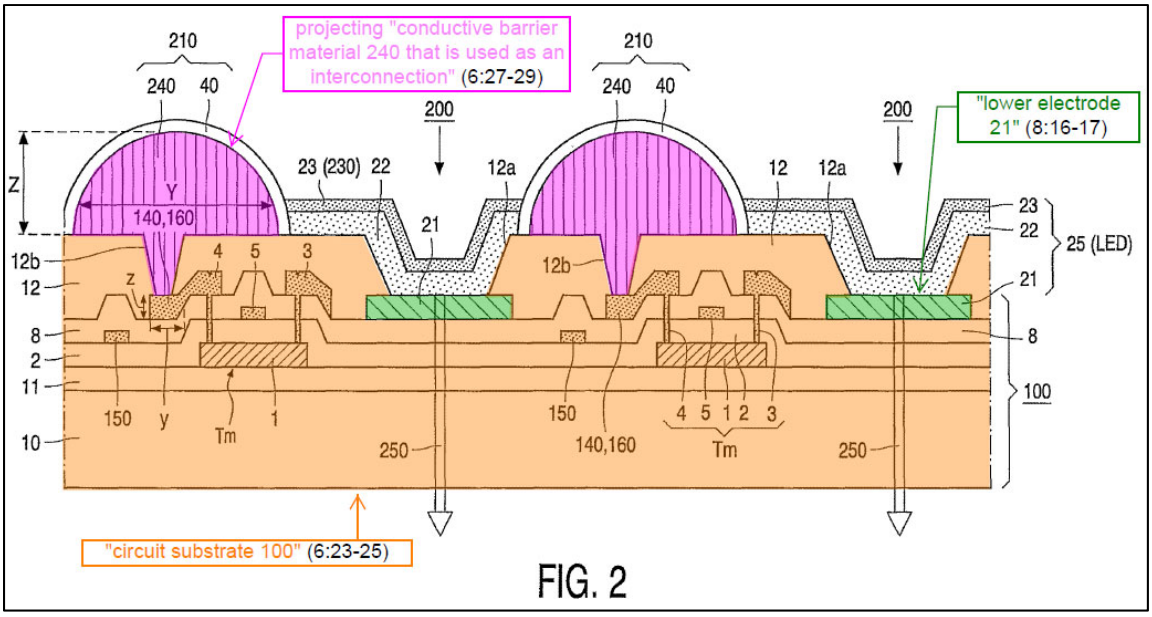


FIG. 2

"comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain"

Childs discloses that "[e]ach pixel 200 comprises" both a "drive TFT T1" and an "addressing TFT T2," Ex. 1005, 7:10–30, as illustrated by annotated Figure 1, Ex. 1018, ¶ [0169]:

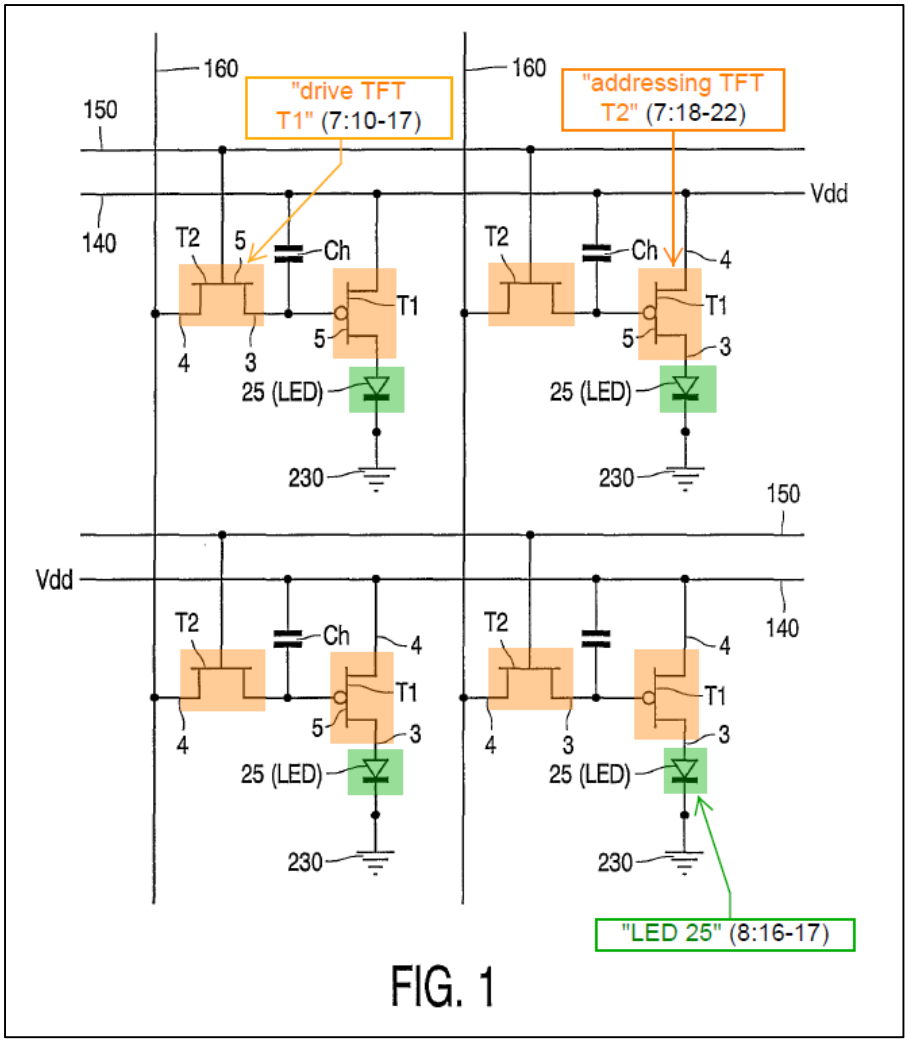


FIG. 1

Annotated Figure 2 of Childs illustrates that each of these transistors T1 and T2 ("Tm") in "circuit substrate 100" comprises an "active semiconductor layer 1" with "source and drain regions" (connected to "electrodes 3 and 4"), "gate electrode 5," and "a gate dielectric layer 2" (the claimed "gate insulating film"), Ex. 1005, 8:3–15; Ex. 1018, ¶ [0170]:

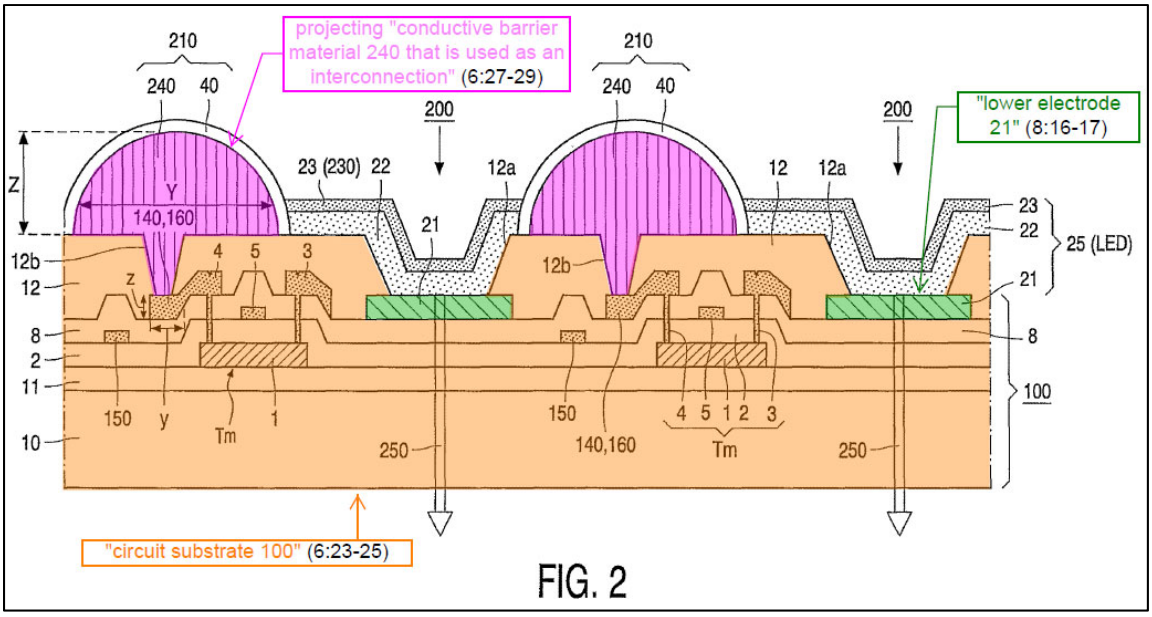


FIG. 2

1[b]: "a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other;"

Childs discloses that its "physical barriers 210" "are constructed with conductive barrier material 240 that is used as an ***interconnection***." Ex. 1005, 6:25–29 (emphasis added). These conductive barriers 240 are "deposited on the insulating layer 12," *id.*, 15:9–23, project from the surface of insulating layer 12 (i.e., from the claimed "surface of the transistor array substrate"), and are arrayed in parallel to each other, as illustrated by annotated Figure 2, Ex. 1018, ¶ [0172]:

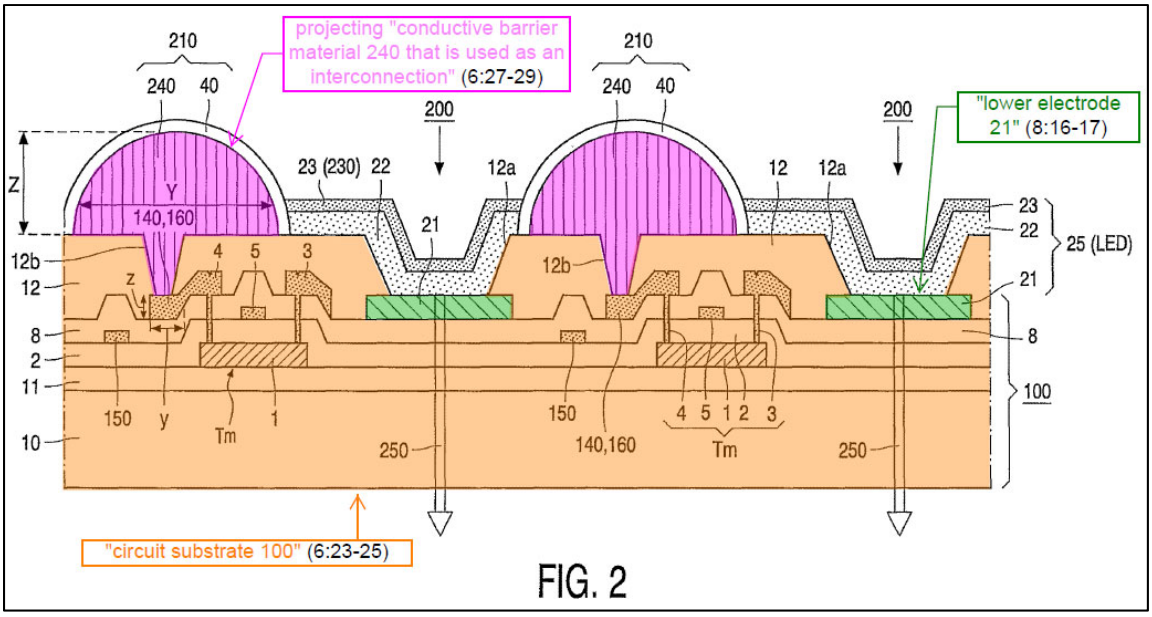


FIG. 2

Childs explains that these "conductive barrier[s] 240" are each "connected to and/or from one or more circuit elements of the circuit substrate 100," such as "supply line 140," "addressing line 150," and/or "signal line 160," Ex. 1005, 9:20–29, and that their "line resistance can be significantly reduced by using the conductive material 240 to replace or back up the conductor line 150 of the circuit substrate," *id.*, 10:25–27. The parallel arrangement of conductive barriers 240 also serves to "separate and prevent overflow . . . between the respective areas of the individual pixels 200 . . . during the provision of [electroluminescent] polymer layers 22." *Id.*, 9:3–11; Ex. 1018, ¶ [0173].

1[c]: "a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate;"

Childs teaches or suggests the elements of this limitation.

"a plurality of pixel electrodes for the plurality of pixels, respectively"

Childs discloses "lower electrode[s] 21" for each pixel 200, Ex. 1005, 8:16–27, which correspond to the claimed "plurality of pixel electrodes for the plurality of pixels." Childs discloses that "[e]ach pixel 200 comprises a current-driven electroluminescent display element 25 (21, 22, 23)," *id.*, 7:10–12, each of which includes "a lower electrode 21" that serves as an anode, *id.*, 8:16–27; Ex. 1018, ¶ [0176].

"the pixel electrodes being arrayed along the interconnections between the interconnections"

Childs further discloses that its pixel electrodes are arrayed along and between the interconnections. Each of the lower electrodes 21 (the claimed pixel electrodes) are arrayed along and between conductive barriers 240 (the claimed interconnections), as illustrated in annotated Figure 2, Ex. 1018, ¶ [0177]:

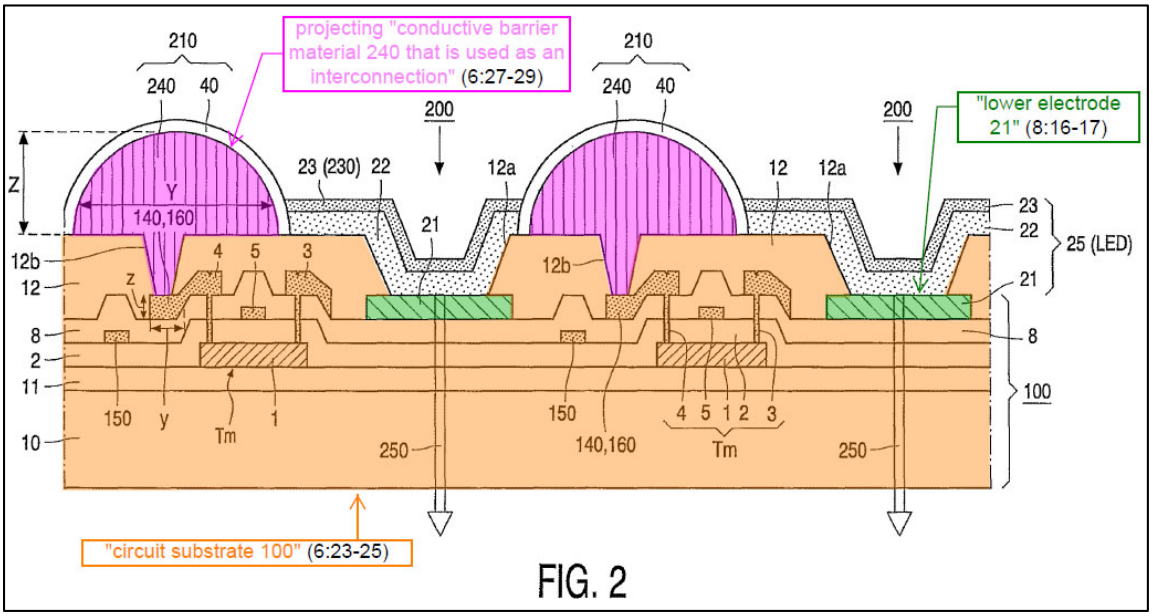


FIG. 2

"the pixel electrodes being arrayed . . . on the surface of the transistor array substrate"

Childs discloses that the lower electrodes 21 are formed on insulating layer 8 and exposed in "connection windows 12a" (i.e., trenches). Ex. 1005, 8:3–27. Accordingly, lower electrodes 21 are located on the surface of the topmost insulating layer of circuit substrate 100 (i.e., insulating layer 8) in these windows (and thus located on the surface of the claimed transistor array substrate), as seen in Figure 2, *id.*; Ex. 1018, ¶ [0178]:

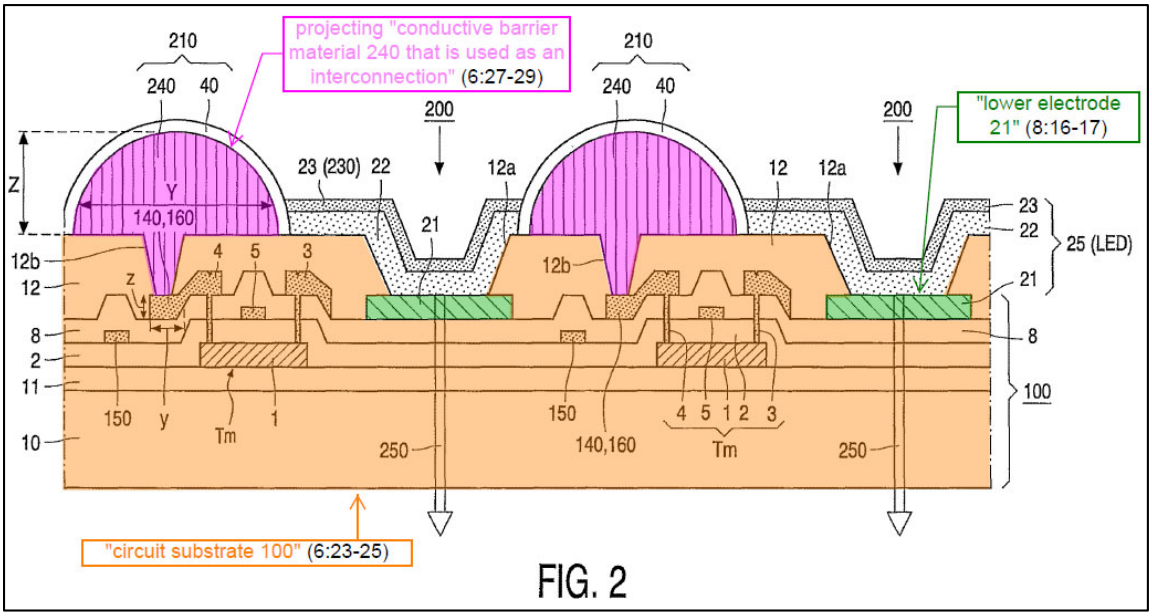


FIG. 2

Additionally, to the extent that there is any question whether lower electrode 21 of Childs is arrayed "on the surface of the transistor array substrate" (e.g., because lower electrode 21 is not on top of the insulating layer 12 which covers aluminum electrodes 3 and 4), it would have been obvious to form lower electrode 21 on the surface of an insulating layer that covers these electrodes 3 and 4. A POSA would

have recognized that this straightforward modification to Childs may have been accomplished in one of two routine ways. Ex. 1018, ¶ [0179].

One option would be to form an additional transparent insulating layer on top of aluminum electrodes 3 and 4, with lower electrode 21 then formed on top of that additional insulating layer (i.e., on the surface of the transistor array substrate). Alternatively, lower electrode 21 may be formed on top of planar insulating layer 12 (instead of on the exposed surface of insulating layer 8).[7] This alternative would

[7] Childs states that the "planar insulating layer 12" can be made "for example of silicon nitride," Ex. 1005, 8:24–27, but also repeatedly discloses that transparent "silicon dioxide" can be used as an alternative "insulating material" to SiN, *id.*, 15:24–28, 16:21–24. Forming "planar insulating layer 12" out of transparent silicon dioxide would allow light emitted by the OLED elements to pass through planar insulating layer 12 when pixel electrodes 21 were formed on its surface. Ex. 1018, ¶ [0187].

merely have required reordering the steps of Childs' fabrication process.[8] Ex. 1018, ¶ [0180].

As described in this petition and the Fontecchio declaration, forming the pixel electrodes of an OLED on top of an insulating layer that covers the metal source and drain electrodes (instead of on the same layer as those metal source and drain electrodes) was a well-known and obvious manufacturing technique at the time of the alleged invention of the '338 patent, as illustrated by other contemporary prior art such as Kobayashi (see above) and U.S. Patent Application Pub. No. 2003/0127657 ("Park") (Ex. 1014). Ex. 1018, ¶¶ [0181]–[0183] (citing Exs. 1003, 1009, 1014); *KSR*, 550 U.S. at 421 ("where . . . there are a finite number of identified,

[8] Because Childs' conductive barriers 240 are so thick, forming the lower electrode 21 on top of planar insulating layer 12 would not have affected those barriers' ability to separate and contain the [electroluminescent] polymer layers 22, due to Childs' thick conductive barriers 240. Ex. 1005, 9:3–11, Fig. 2. And Childs notes that barriers 210 may be made even thicker, Ex. 1005, 10:25–11:2 (describing the barrier thickness as "at least" as thick as the provided examples)—or a shallow window could be etched in planar insulating layer 12 before forming the lower electrode 21, using the "known . . . photolithographic masking and etching" techniques described by Childs, *id.*, 14:29–15:2; Ex. 1018, ¶¶ [0192]–[0193].

predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp").

The contemporary prior art also provided an express motivation for forming such an insulating layer over the metal source and drain electrodes (for example, a planarization layer) before forming the anode electrodes of the OLED pixels. U.S. Patent Application Pub. No. 2002/0000576 ("Inukai") (Ex. 1016) noted that forming an "interlaying insulating film" on top of an OLED's TFT array would provide "a good, level surface" for the OLED elements, which can be "extremely sensitive to unevenness" Ex. 1014, ¶¶ [0310]–[0311], Fig. 14; Ex. 1018, ¶ [0184]. U.S. Patent Application Pub. No. 2002/0009538 ("Arai") (Ex. 1017) similarly explained that "[i]t is very important" and "desirable" to form a level insulating layer above the TFT array of an OLED "before forming the pixel electrode so that the light-emitting layer can be formed on as flat [of a] surface as possible." Ex. 1017, ¶ [0077], Fig. 5B; Ex. 1018, ¶ [0185].

Further, as discussed by Dr. Fontecchio, making either of these obvious design choices would have actually simplified the manufacturing process of Childs. Lower electrode 21 ("an anode of indium tin oxide") would no longer need to be fabricated in the same layer as "metal electrodes 3 and 4 (typically of aluminum)." Ex. 1005, 8:3–8, 8:19–22. The intervening insulating layer would thus serve to protect the aluminum electrodes 3 and 4 from additional etching or oxygen

contamination during the formation of the transparent indium tin oxide electrode 21, preventing the formation of non-conductive aluminum oxide on electrodes 3 and 4 and simplifying the manufacturing process. Ex. 1018, ¶¶ [0188]–[0191].

Accordingly, making such a change to Childs' manufacturing process would have been an obvious design choice well known in the art and well within the knowledge and skill of a POSA at the time of the alleged invention of the '338 patent, as evidenced by the Kobayashi, Park, Inukai, and Arai prior art references discussed above, each of which disclosed forming the OLED pixel electrode on top of a planar insulating layer. This change would have required little more than a straightforward change to the photomasks used to fabricate the TFT array in order to create "windows" through that planar insulating layer that would connect the TFT array to the OLED elements (just as conductive barriers 240 are already connected to elements within the circuit substrate 100 via windows 12b). Childs itself notes that the "[c]onnection windows (such as vias 12a, 12b, 12x, etc.) are opened in the layer 12 ***in known manner***, for example by photolithographic masking and etching." Ex. 1005, 14:29–15:2 (emphasis added); Ex. 1018, ¶ [0186].

1[d]: "a plurality of light-emitting layers formed on the pixel electrodes, respectively; and"

Childs discloses a plurality of light-emitting layers formed on the pixel electrodes, respectively. As noted above, Childs discloses that "[e]ach pixel 200 comprises a current-driven electroluminescent display element 25 (21, 22, 23)," Ex.

1005, 7:10–12, and that "a light-emitting organic semiconductor material 22" is formed "between" each "lower electrode 21 and an upper electrode 23," *id.*, 8:16–27, as depicted in Fig. 2, Ex. 1018, ¶¶ [0194]–[0195]. *See also* Ex. 1005, 9:3–11 (discussing the organic semiconducting polymer used to create "electroluminescent layers 22"), 15:29–31.

1[e]: "a counter electrode which is stacked on the light-emitting layers,"

Childs discloses a counter electrode which is stacked on the light-emitting layers. As noted above, Childs discloses that "[e]ach pixel 200 comprises a current-driven electroluminescent display element 25 (21, 22, 23)," Ex. 1005, 7:10–12, that "a light-emitting organic semiconductor material 22" is formed "between" each "lower electrode 21 and an upper electrode 23," *id.*, 8:16–27, and that "the upper electrode 23 may be a cathode," *id.*, 8:19–22; Ex. 1018, ¶ [0197].

1[f]: "wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period."

Childs discloses that the plurality of transistors for each pixel include the claimed "driving transistor" and "switch transistor," and it would have been obvious to further incorporate the claimed "holding transistor" in view of Shirasaki.

Specifically, Childs discloses a "drive TFT T1" "connected in series" with LED 25 (the claimed "driving transistor, one of which the source and the drain of which is connected to the pixel electrode") and an "addressing TFT T2" connected "to the gate of the individual drive TFT T1 of the respective pixel" (the claimed "switching transistor which makes a write current flow between the drain and the source of the driving transistor"), Ex. 1005, 7:10–30, as illustrated by annotated Figure 1 of Childs, Ex. 1018, ¶ [0201]:

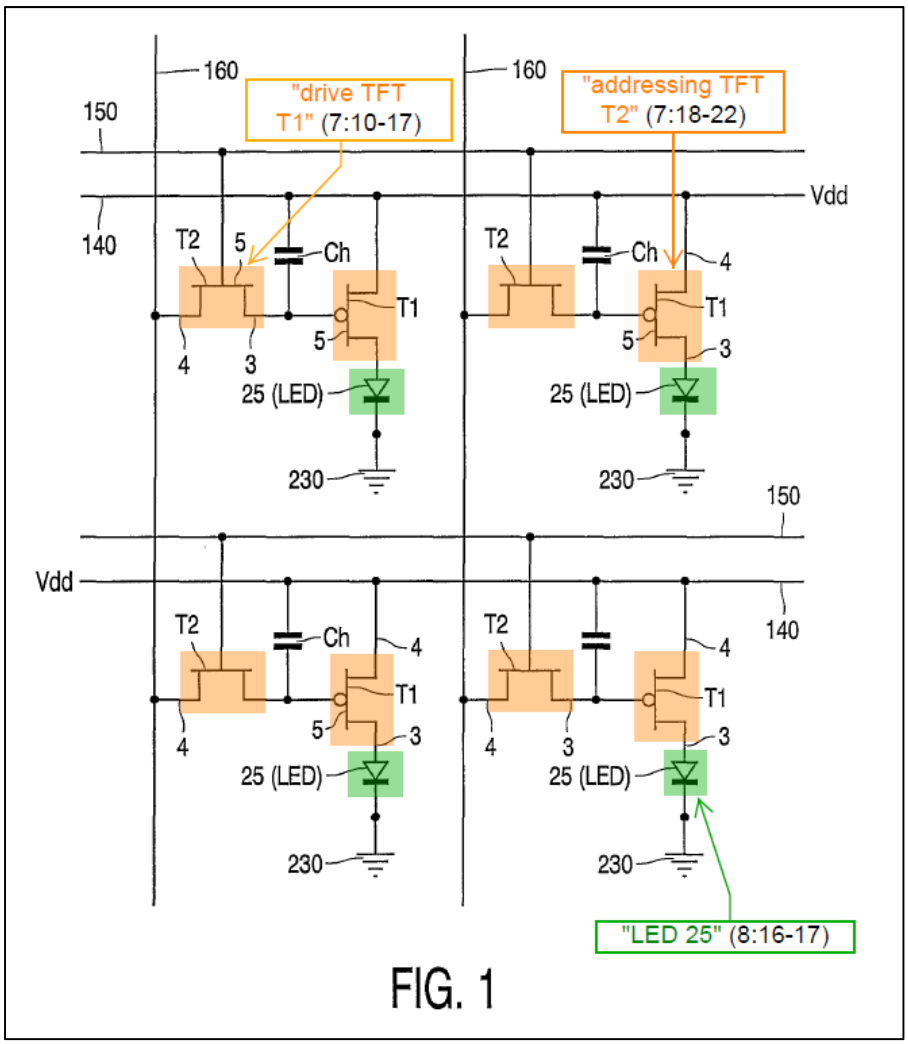
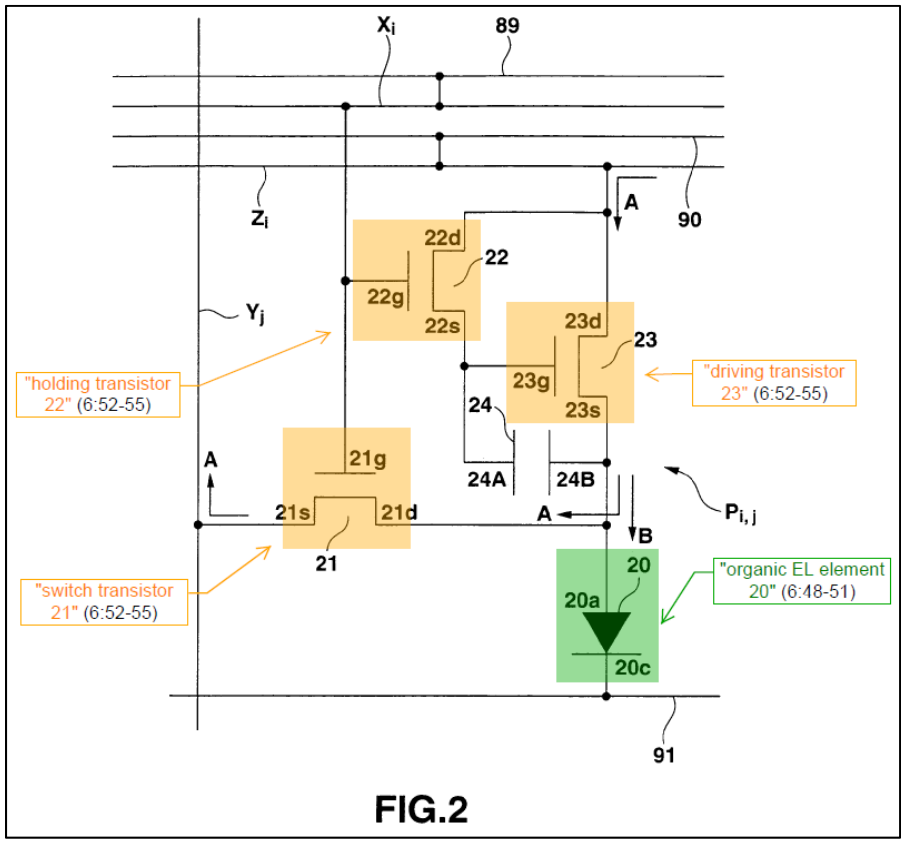
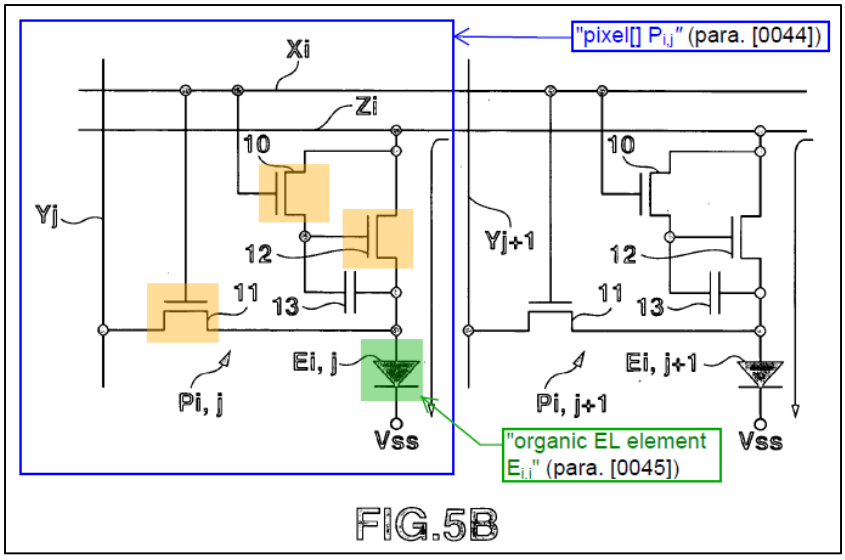


FIG. 1

Childs does not include a "holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period," as recited by claim 1. However, this "holding transistor" limitation would have been obvious based on Shirasaki, which disclosed replacing a two-transistor pixel circuit (as in Childs) with a three-transistor pixel circuit that includes each of the claimed "driving transistor," "switching transistor," and "holding transistor." In fact, Shirasaki's figures illustrate the same three-transistor pixel circuit that was later depicted in the figures of the '338 patent, Ex. 1018, ¶¶ [0202]–[0204]:



Ex. 1001 ('338 patent), Fig. 2 (annotated).



Ex. 1004 (Shirasaki), Fig. 5B (annotated).

Motivation to Combine:

Childs and Shirasaki both disclose TFT pixel circuits for use in AMOLED display panels. And Shirasaki provides an express teaching, suggestion, or motivation for why a POSA would have replaced Childs' two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit, as discussed above in § VIII.A.1.1[f] regarding Shirasaki's discussion of such two-transistor pixel circuits. *See* Ex. 1004, ¶¶ [0003]–[0004], [0007] ("it is difficult to display images with a desired luminance tone for long time periods . . . As a consequence, no accurate tone control can be performed . . . it becomes more difficult to make the characteristics of the transistors 104 of the individual pixels uniform"); Ex. 1018, ¶¶ [0205]–[0206].

Accordingly, by replacing the two-transistor pixel circuit of Childs with Shirasaki's three-transistor pixel circuit, Shirasaki explained that several advantages

can be obtained.[9] Ex. 1001, ¶ [0018] ("This suppresses the influence of variations in the voltage-current characteristic of the control system and allows the optical element to stably display images with desired luminance"), ¶ [0011] ("[O]ne advantage of the present invention is that pixels stably display image with desired luminance in a display panel."); Ex. 1018, ¶¶ [0207]–[0208].[10]

For at least these reasons, the prior art provided a teaching, suggestion, or motivation to replace Childs' two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit. This replacement would merely have been the "simple substitution of one known element [Shirasaki's three-transistor pixel circuit] for

[9] While Childs' pixel circuit includes "a holding capacitor Ch" (depicted above) that "hold[s] the resulting conductive state of the drive TFT T1," Ex. 1005, 7:23–39, this capacitor does not provide the same advantages as Shirasaki's "holding transistor"—the pixel circuits of both Shirasaki and the '338 patent still include a capacitor in addition to the "driving," "switch," and "holding" transistors, Ex. 1004, Figs. 1, 5A–B; Ex. 1001, Fig. 2; Ex. 1018, ¶¶ [0208].

[10] Shirasaki also explains why a POSA would have been motivated to use a three-transistor pixel circuit instead of a pixel circuit with "four or more transistors in one pixel," Ex. 1004, ¶ [0009], as discussed above in § VIII.A.1.1[f]; Ex. 1018, ¶ [0209] (citing Ex. 1004, ¶¶ [0012], [0019], [0020]).

another [Childs' two-transistor structure]," and would have required no more than "the predictable use of prior art elements according to their established functions." *KSR*, 550 U.S. at 415–19; Ex. 1018, ¶ [0210].

Reasonable Expectation of Success:

Replacing Childs' two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit would have been well within the skill of a POSA. As discussed above, Shirasaki expressly discloses that its three-transistor pixel circuit is meant to replace the two-transistor pixel circuit found in "conventional light emitting element display" devices (such as Childs), and would have given a POSA a reasonable expectation of success in modifying Childs in this manner. Ex. 1004, ¶¶ [0002]–[0008], [0013]–[0019]. And Childs and Shirasaki each come from the same field of endeavor—active matrix organic light-emitting diode display panels featuring thin-film transistor arrays. Ex. 1005, 1:5–7; Ex. 1004, ¶¶ [0041], [0043]; Ex. 1018, ¶¶ [0211]–[0212].

Accordingly, a POSA would have recognized that the two-transistor pixel circuit in Childs could be replaced with Shirasaki's three-transistor pixel circuit without altering any of the layers above the transistor array substrate in Childs' layered OLED structure. Childs itself confirms that:

> ***Other pixel circuit configurations are known for active matrix display devices***, and it should be readily understood that the present invention

may be applied to the pixel barriers of such a device ***regardless of the specific pixel circuit configuration of the device.***

Ex. 1005, 7:6–9 (emphasis added). Making this modification would have required no more than the "simple substitution of one known element [Shirasaki's three-transistor pixel circuit] for another [Childs' two-transistor structure],"[11] and would have required simply "the predictable use of prior art elements according to their established functions." *KSR*, 550 U.S. at 415–19; Ex. 1018, ¶¶ [0213]–[0214].

2. Claim 2

"A panel according to claim 1, wherein said plurality of interconnections include at least one of a feed interconnection connected to the other of the source and the drain of at least one of the driving transistors, a select interconnection which selects at least one of the switch

[11] While making the change from Childs' two-transistor pixel circuit to Shirasaki's three-transistor pixel circuit would have required changing the photomasks used to fabricate the TFT array and relocating the "windows" through Childs' "planar insulating layer 12" that connect the TFT array to the OLED elements, these were routine and predictable manufacturing steps involved during the fabrication of every OLED display panel. As Childs notes, the "[c]onnection windows (such as vias 12a, 12b, 12x, etc.) are opened in the layer 12 ***in known manner***, for example by photolithographic masking and etching." Ex. 1005, 14:29–15:2 (emphasis added). Ex. 1018, ¶ [0215].

transistors, and a common interconnection connected to the counter electrode."

In light of the disclosure and claims of the '338 patent, a POSA would have understood this claim to require that the plurality of interconnections include at least one of the three types of claimed interconnections ("feed," "select," or "common") (as opposed to requiring all three types of claimed interconnections, as recited by dependent claim 4). Ex. 1018, ¶ [0216]. And Childs' interconnections constitute feed interconnections connected to the other of the source and the drain of at least one of the driving transistors. Childs discloses that its "conductive barrier[s] 240" can be "connected to and/or from one or more circuit elements," with one of those circuit elements being the "supply line 140," Ex. 1005, 9:20–29, which is itself connected to drive TFT T1, *id.*, 7:10–17, as depicted in Figure 1 of Childs, Ex. 1018, ¶ [0217]:

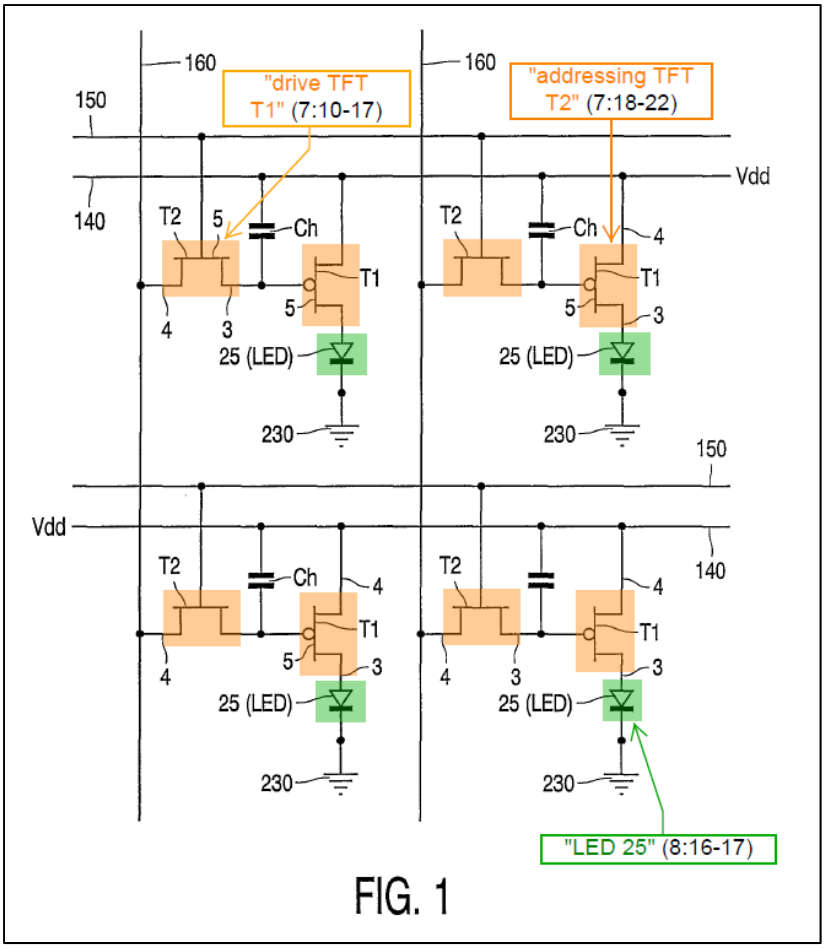


FIG. 1

Childs' interconnections also constitute select interconnections which select at least one of the switch transistors. Childs discloses that "conductive barrier[s] 240" can supplement and/or replace "addressing line 150," Ex. 1005, 9:20–29, which transmits the "selection signal" that "turns on the addressing TFT T2," *id.*, 7:18–22, as illustrated in Figure 1, above, Ex. 1018, ¶ [0218].

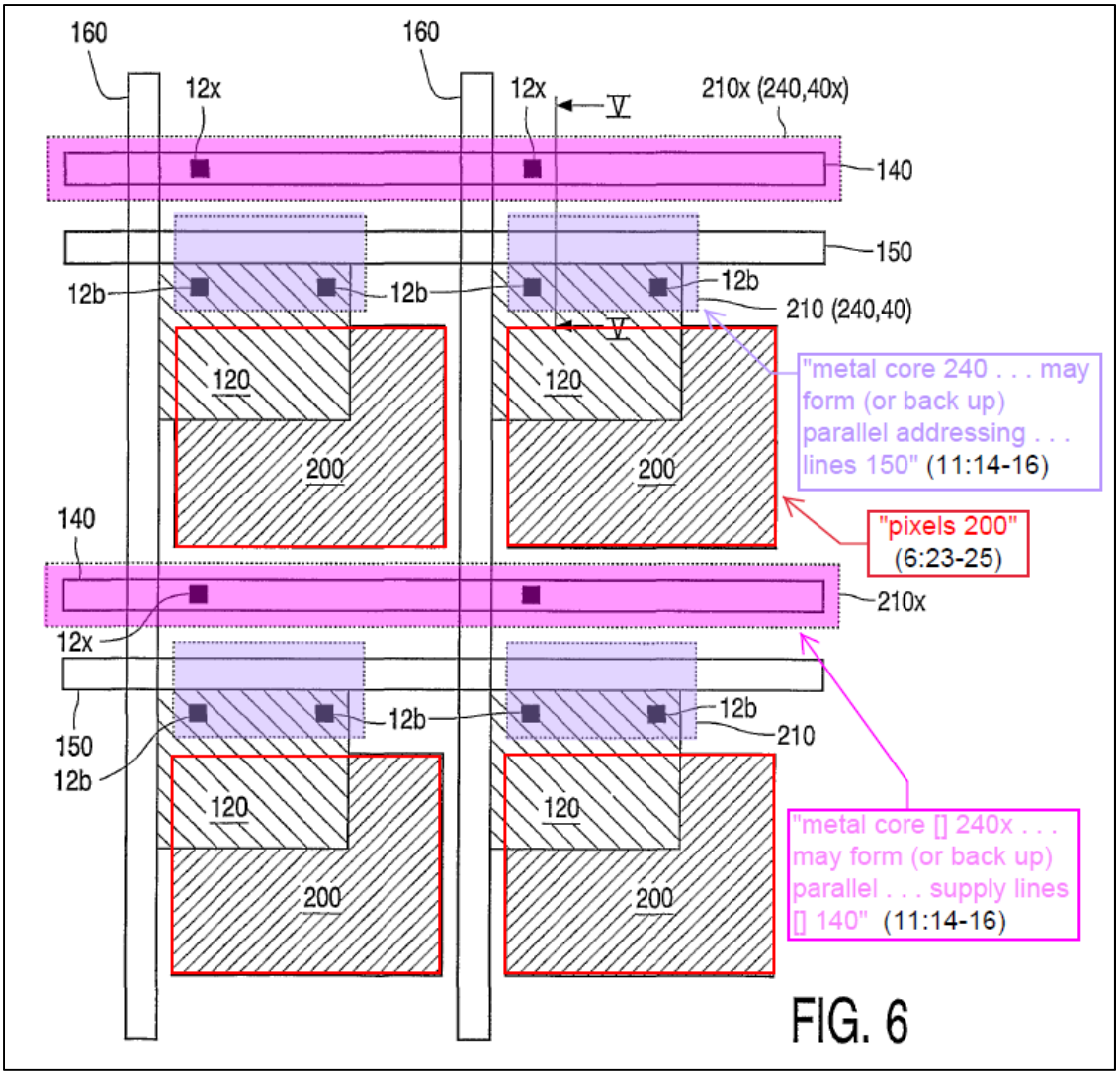
3. Claim 3

"A panel according to claim 2, wherein each of the light-emitting layers is formed between two of the feed

interconnection, the select interconnection, and the common interconnection."

Childs discloses embodiments in which each of the light-emitting layers is formed between a feed interconnection and a select interconnection.

As illustrated in Figure 1, Childs' pixels are each bounded on one side by voltage supply line 140, and on the other side by addressing line 150. And, for example, Childs discloses that a first "metal core 240" of a first "barrier 210" "form[s] (or back[s] up)" "addressing line 150," (the claimed select interconnection) and a second "metal core 240x" of a second "barrier 210x" "form[s] (or back[s] up)" "supply line 140" (the claimed feed interconnection). Ex. 1005, 11:11–21. This is illustrated in Figs. 5–6 of Childs, which show pixels 200 (each of which features organic light-emitting layers, as discussed above) formed between the projecting interconnections 210 (on top) and 210x (on bottom), Ex. 1018, ¶¶ [0220]–[0221]:



4. Claim 5

"A panel according to claim 1, wherein said plurality of pixels include a red pixel, a green pixel, and a blue pixel."

Childs teaches, or at a minimum strongly suggests, this limitation. Childs states that its barriers "prevent pixel overflow of conjugate polymer materials that may be ink-jet printed for red, green and blue pixels of a color display." Ex. 1005, 1:20–2:1. Accordingly, a POSA would have recognized that Childs was directed for

use in a conventional color OLED display, which were well known to require and include red, green, and blue pixels. Ex. 1018, ¶ [0223] (citing Ex. 1007).

5. Claim 6

"A panel according to claim 5, wherein said plurality of pixels comprises a plurality of sets each including the red pixel, the green pixel, and the blue pixel arrayed in an arbitrary order."

Childs states that its barriers "prevent pixel overflow of conjugate polymer materials that may be ink-jet printed for red, green and blue pixels of a color display," Ex. 1005, 1:20–2:1, and a POSA would have recognized that these red, green, and blue pixels would be arrayed into sets of three pixels each including a red, green, and blue pixel in an arbitrary order, as disclosed by numerous contemporary prior art references that discussed color OLED displays, Ex. 1018, ¶ [0225] (citing Ex. 1007).

6. Claim 7

"A panel according to claim 1, wherein at least one of the interconnections has a thickness of 1.31 to 6.00 μm."

Childs discloses that "the conductive barrier material 240" (the claimed interconnections) "may have a thickness Z," disclosing (in the only example provided) that "Z may be between 2 μm and 5 μm," Ex. 1005, 10:30–11:2, within the claimed range, Ex. 1018, ¶ [0227].

7. Claim 8

"A panel according to any one of claims 1 or 2 to 7, wherein at least one of the interconnections has a width of 7.45 to 44.00 µm."

Childs discloses that "the conductive barrier material 240" (the claimed interconnections) "may have a line width Y," disclosing (in the only example provided) that "Y may be 20µm," Ex. 1005, 11:3–6, within the claimed range, Ex. 1018, ¶ [0228].

8. Claim 9

"A panel according to claim 1, wherein at least one of the interconnections has a resistivity of 2.1 to 9.6 µΩcm."

As explained by Kobayashi, the resistivity of the interconnections depends on the material used to construct them (as opposed to the geometry and/or dimensions of those interconnections), Ex. 1018, ¶ [0229] (citing Ex. 1003). Childs discloses preferably using either "aluminium or copper" as the "electrically conductive material 240" used to construct its interconnections. Ex. 1005, 10:6–10, 16:27–28. And the '338 patent itself states that the interconnections will have a "resistivity of 2.1 to 9.6 µΩcm" "when an Al-based material or Cu is used" to construct those interconnections. Ex. 1001, 21:58–62; Ex. 1018, ¶ [0229].

9. Claim 10

"A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer that is different from a layer forming the source and the drain of

each of the transistors and a layer forming the gate of the transistors."

Childs discloses that its "conductive metal barriers 240" (the claimed plurality of interconnections) are formed from a conductive layer that is different from the layer 1 forming the source and the drain of each of the transistors, and the layer 5 forming the gate of each of the transistors, Ex. 1005, 8:3–15, 10:6–10, as illustrated by annotated Figure 2, Ex. 1018, ¶ [0231]:

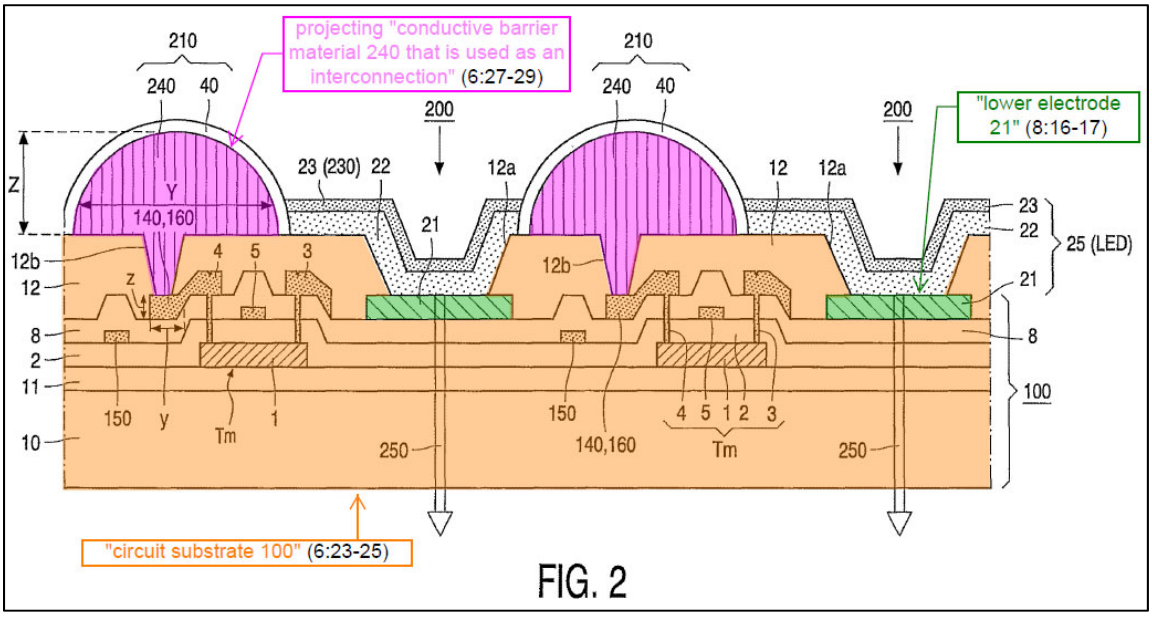


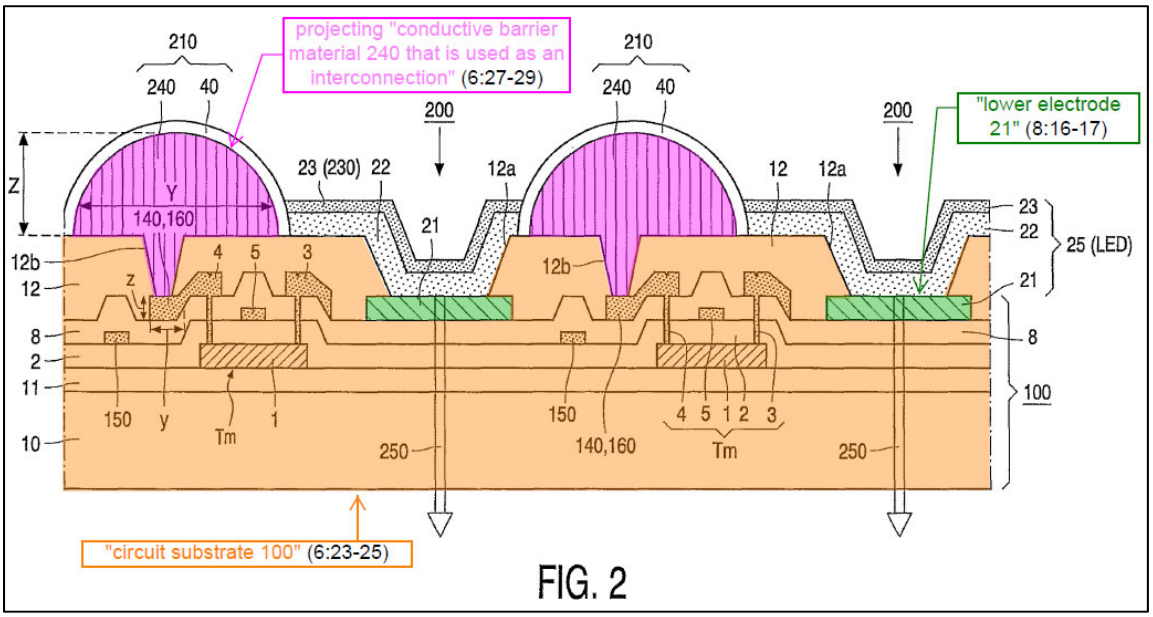
FIG. 2

Childs further discloses that the source and drain regions 1 are made from polysilicon, and that the gate electrode 5 is made from aluminum or polysilicon, Ex. 1005, 8:3–8, whereas the conductive metal barriers 240 are made from metal with "very low resistivity," such as "aluminum or copper or nickel or silver," *id.*, 10:6–8; Ex. 1018, ¶ [0232].

10. Claim 11

"A panel according to claim 1, wherein said plurality of interconnections are formed from a conductive layer different from a layer forming the pixel electrodes."

Childs discloses that its "conductive metal barriers 240" (the claimed plurality of interconnections) are formed from a conductive layer that is different from the layer forming the pixel electrodes 21, as illustrated by annotated Figure 2, Ex. 1018, ¶ [0234]:

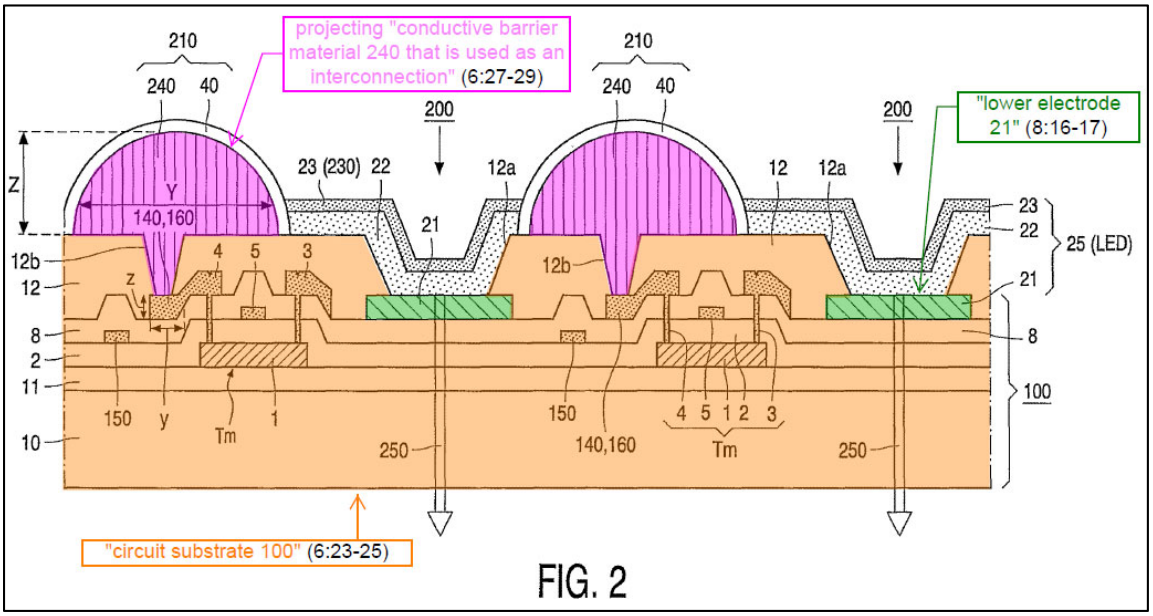


Childs discloses that lower electrode 21 "may be an anode of indium tin oxide (ITO)," Ex. 1005, 8:19–22, whereas the conductive metal barriers 240 are made from metal with "very low resistivity," such as "aluminum or copper or nickel or silver," *id.*, 10:6–8; Ex. 1018, ¶ [0235].

11. Claim 12

"A panel according to claim 1, wherein said plurality of interconnections are thicker than a layer forming the source and the drain of each of the transistors and a layer forming the gate of each of the transistors."

Childs expressly states that its "conductive barrier material 240"—the claimed plurality of interconnections—"may have a thickness Z that is a factor of two or more (for example at least five times) larger than the thickness z of this conductor layer 5(150)," which forms the gate of each of the transistors "in the circuit substrate 100." Ex. 1005, 10:30–11:1. And annotated Figure 2 of Childs, for example, illustrates how conductive metal barriers 240 (the claimed plurality of interconnections) are substantially thicker than both layer 1 that forms the source and drain of each of the transistors, as well as layer 5 that forms the gate of each of the transistors, Ex. 1018, ¶¶ [0237]–[0238]:



12. Claim 13

"A panel according to claim 1, wherein said plurality of interconnections are thicker than the pixel electrodes."

Childs expressly states that its "conductive barrier material 240 may have a thickness Z that is a factor of two or more (for example at least five times) larger than the thickness z of this conductor layer 5(150) in the circuit substrate 100," Ex. 1005, 10:30–11:1, whereas the "lower electrode 21 is formed as a thin film," *id.* 8:22–24. And annotated Figure 2 of Childs, for example, illustrates how the conductive metal barriers 240 (the claimed plurality of interconnections) are substantially thicker than layer 21 that forms the pixel electrodes of Childs' OLED pixels 200, Ex. 1018, ¶¶ [0239]–[0240]:

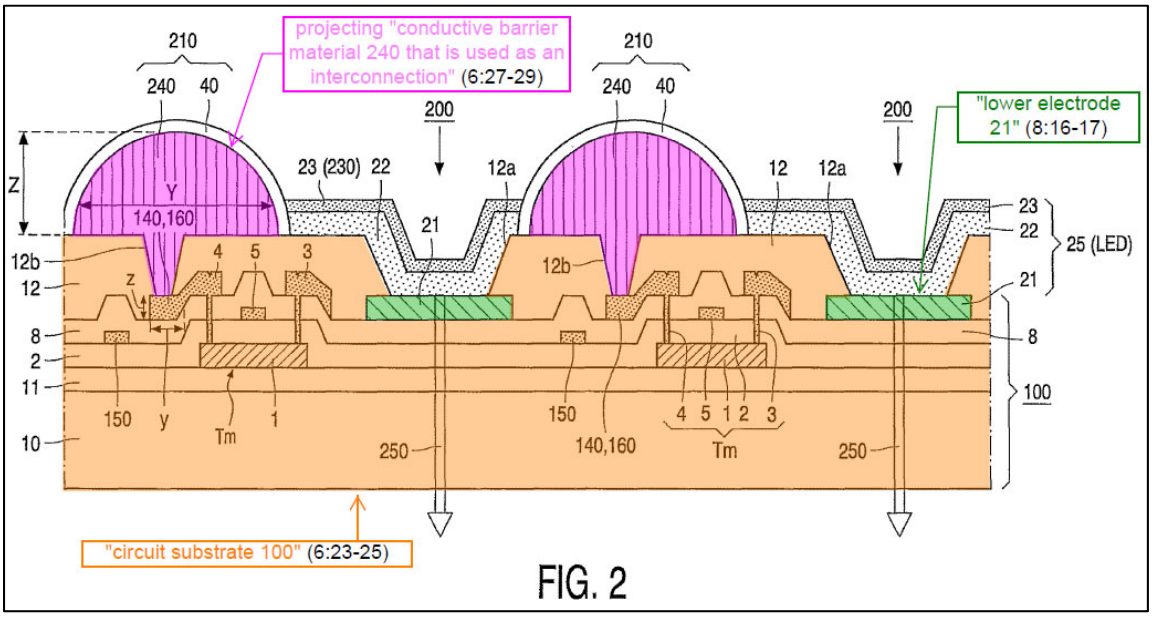


FIG. 2

IX. CONCLUSION

Petitioner respectfully requests *inter partes* review and cancellation of claims 1–3 and 5–13 of the ’338 patent.

Date: December 18, 2019

Respectfully submitted,

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CERTIFICATION UNDER 37 C.F.R. § 42.24(D)

I certify that the foregoing complies with the type-volume limitation of 37 C.F.R. § 42.24 and contains 13,946 words based on the word count indicated by the word-processing system used to prepare the paper, and excluding those portions exempted by § 42.24(a).

Date: December 18, 2019

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6 and 42.105, I certify that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,446,338 Under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq.*, together with Petitioner's Exhibits Nos. 1001–1019, was served by FedEx, a means at least as fast and reliable as Priority Mail Express®, on the following correspondence address of record for patent owner:

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